A DESIGN TECHNIQUE FOR GAAS MMIC DIFFERENTIAL AMPLIFIERS BASED ON PHYSICAL PARAMETERS OF THE FOUNDRY

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ABSTRACT

This paper presents a simple design technique for differential amplifiers working at frequencies above few GHz, that allows the application of well-known low frequency techniques to microwave circuitry. It is based on the parametrization of the characteristic functions of a differential pair -CMRR and differential gains - in terms of only three design variables: drain resistor R_d, gate width W_1 and normalized bias current $i=I_d/I_{dss}$. A 0.5-6 GHz power divider providing both in-phase power division and gain has been designed using the proposed technique. An amplitude balance ≤ 0.2 dB and a phase balance $\leq 3°$ have been measured. The chip has been designed using the 0.5 µm, F20 process of GEC-Marconi.

I. INTRODUCTION

The differential amplifier is a simple, well-known and versatile circuit structure that has many applications in a wide range of electronic systems, but it is rare to find them working at microwave frequencies above a few GHz. Although the bipolar-transistor version is normally used at low-frequency analog electronic and its theoretical analysis is plentiful in the literature [1]. However, MMIC GaAs MESFET structure still has not been sufficiently studied and presents some differences with respect to the bipolar version [2]. However, MMIC technology allows to design and fabricate circuits, using a source-coupled GaAs MESFET differential amplifier as key element in microwave frequency range. Recent MMIC applications using differential amplifiers include high-speed GaAs integrated circuits [3], frequency doublers [4], active splitters with an arbitrary phase relationship [5], baluns for double blanced mixers [6] and linear vector modulators [7].

This paper presents a simple design technique for GaAs MESFET differential amplifier circuit structure, that allows the application of well-known low frequency techniques to microwave circuitry thanks to MMIC implementation. The developed technique is based on the analytic expressions for the differential gain and the Common Mode Rejection Ratio (CMRR). Former expressions are first obtained in terms of the elements of the GaAs MESFET small-signal equivalent circuit. On other hand, foundries normally provide polynomial functions for the elements of the equivalent circuits. These functions describe the elements the element variation with respect to two variables, normally, the gate width (W) and the bias current normalized to the saturation one ($i=I_d/I_{dss}$). On this way, the differential gains and the CMRR can be obtained in terms of only three design variables: drain resistor (R_d), gate width (W) and normalized bias current ($i=I_d/I_{dss}$). The design procedure lies in eliminating one of these three variables by imposition of auxiliary design condition and to represent graphically the characteristic functions in terms of the other two varaibles. On this way, the optimal values of the design variables can be found by imposing the specifications of the circuit on those curves. The developed technique has been applied to the F20 process of GEC-Marconi.

II. THEORETICAL ANALYSIS

Figure 1, depicts the schematic of a GaAs MESFET differential pair structure with drain passive loads, the current source is implemented with a GaAs MESFET biased at 100% saturation current (I_{dss}). To analyse the GaAs MESFET differential pair structure, a simple small-signal equivalent circuit model has been used, whose schematic is shown in fig.2. The analytic expressions for differential gain and CMRR in terms of the elements of that equivalent circuit are shown in Table I.

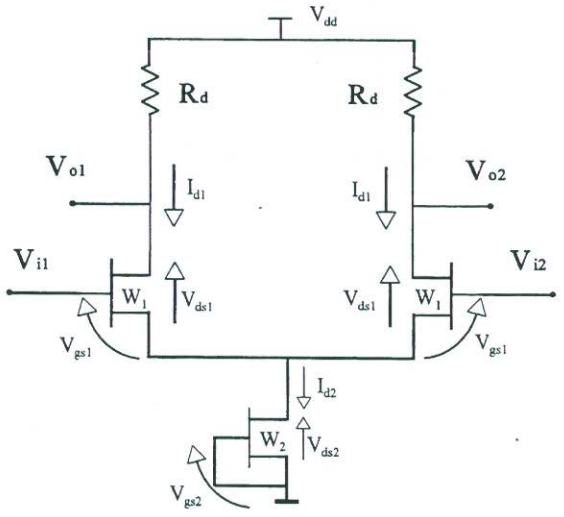

Fig.1. Schematic of a differential amplifier with GaAs MESFETs

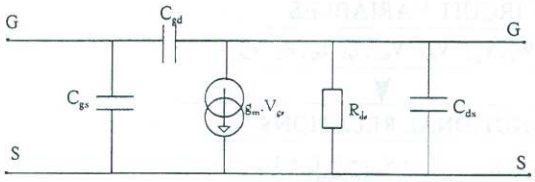

Fig.2. GaAs MESFET simplified equivalent small-signal circuit

TABLE.I Analytic expresions

- *Differential gain*

$$G_d(s) = G_{do}\frac{1+\frac{s}{s_o}}{1+\frac{s}{s_1}}$$

$$G_{do} = -\frac{1}{2}\frac{g_m R_{ds} R_d}{R_{ds}+R_d} \qquad S_o = -\frac{g_m}{C_{gd}} \qquad S_1 = \frac{R_{ds}+R_d}{(C_{ds}+C_{gd})R_{ds}R_d}$$

Common mode rejection ratio -CMRR-

$$CMRR(s) = CMRR_o\frac{\left(1+\frac{S}{S_o}\right)\left(1+\frac{S}{S_{11}}+\frac{S^2}{S_{12}}\right)}{\left(1+\frac{S}{S_1}\right)\left(1+\frac{S}{S_{o1}}+\frac{S^2}{S_{o2}}\right)}$$

$$CMRR_o = \frac{1}{2}\left[1+\frac{2R_s}{R_{ds}+R_d}(1+g_m R_{ds})\right]$$

$$S_{o1} = -\frac{g_m R_{ds}}{C_{gd}[R_{ds}+2R_s(1+g_m R_{ds})]+2C_{gs}R_s}$$

$$S_{o2} = \frac{g_m}{2R_s[C_{ds}C_{gd}+C_{gs}(C_{ds}+C_{gd})]}$$

$$S_{12} = \frac{R_{ds}+R_d+2R_s(1+g_m R_{ds})}{2R_s R_{ds}R_d[C_{ds}C_{gd}+C_{gs}(C_{ds}+C_{gd})}$$

$$S_{11} = -\frac{R_{ds}+R_d+2R_s(1+g_m R_{ds})}{R_{ds}R_d(C_{ds}+C_{gd})+2R_s R_{ds}(C_{ds}+C_{gs})+2R_s R_d[C'_{gs}+C_{gs}(1+g_m R_{ds})]}$$

$$with \quad C_{gs} = C_{gs}+\frac{C_s}{2}$$

III. DESIGN TECHNIQUE

The problem of the design of differential pair is to find the variables that characterize the circuit: V_{dd}, R_d, I_d, V_{ds1}, V_{gs1}, I_{d2}, V_{gs2}, V_{ds2}, W_1 and W_2, so that, the imposed specifications are satisfied.

To simplify the analysis and obtain simple equations of design, the following assumptions have been made:

a) The MESFETs currents are independent of its drain-source voltages, so that, they are fixed by the elements of the rest of the circuit.

b) The elements of the small signal equivalent circuit depend only on bias current and width gate, and not on drain source voltage.

The errors introduced by these assumptions are negligible in most cases.

Taking into account the equations of Table I and the closed forms expressions for the elements of equivalent circuit model provide by GEC Marconi Foundry, the characteristic functions, differential gains for common and differential modes and the CMRR, can be obtained in terms of the next design variables: drain resistor (R_d), gate width (W_1) and bias current normalized to the saturation current ($i=I_{d1}/I_{dss}$). This process is shown in the flow chart of fig 3.

The design procedure lies in removal one of these three variables by imposition an auxiliary design condition, for instance, constant differential gain or CMRR at work band or cutoff frequency of differential gain or CMRR equal to upper edge of work band. On this way, the characteristic functions can be graphically represented in terms of the other two variables and the optimal value of the design variables can be found by imposing the specifications of the circuit in those curves. Figures 4 and 5 show the design plots when the design condition is cuttoff frequency of CMMR equal to upper edge of work band. This approach can be used when the circuit works near CMMR's cutoff frequency and it is of interest to fix it over frequency band. The plots have been depicted for a CMRR's cutoff frequency of 3 Ghz as it is shown to maximize the CMRR and the differential gain is better to work with low drain currents.

IV. DESIGN EXAMPLE

A 0.5-6 GHz active power divider providing both in-phase power division and gain has been designed using the developed technique. The circuit consists of three basic subnetworks: a) An input stage in common-gate which matches the circuit input to 50 Ω and supports part of the total gain. The input conductance similar to the MESFET's transconductance, must be selected as close as possible to the characteristic conductance (20 mS), requiring a gate width transistor of 100 µm. b) A cascade of two differential stage, designed according the proposed technique to maximize the CMRR and so that reduce the amplitude and phase errors. The MESFET's gate width of pair branches is 140 µm and the MESFET used as current source is 104 µm. c) Two common source stages which matches each differential pair output to 50 Ω. The circuit was fabricated using the monolithic GEC-Marconi standard F20 process. A micrograph of the IC is shown in fig.6. Chip size is 2,3x2,3 mm. It is comprised of a 9 MESFET, 17 capacitors, 17 resistors and 3 inductors. The different bias voltages are externally introduced so that, bias points may be controlled easily when the circuit is measured.

The IC supply voltage are -0.8V and 8V, and the DC power is equal to 500mW. In figures 7, 8 and 9, a comparison between experimental and simulated results are shown for output amplitude and phase errors, input and output matching and transmission losses, respectively, are shown. An amplitude and phase balance better than 0.2 dB and 3° and input and output matching better than 20 dB have been measured.

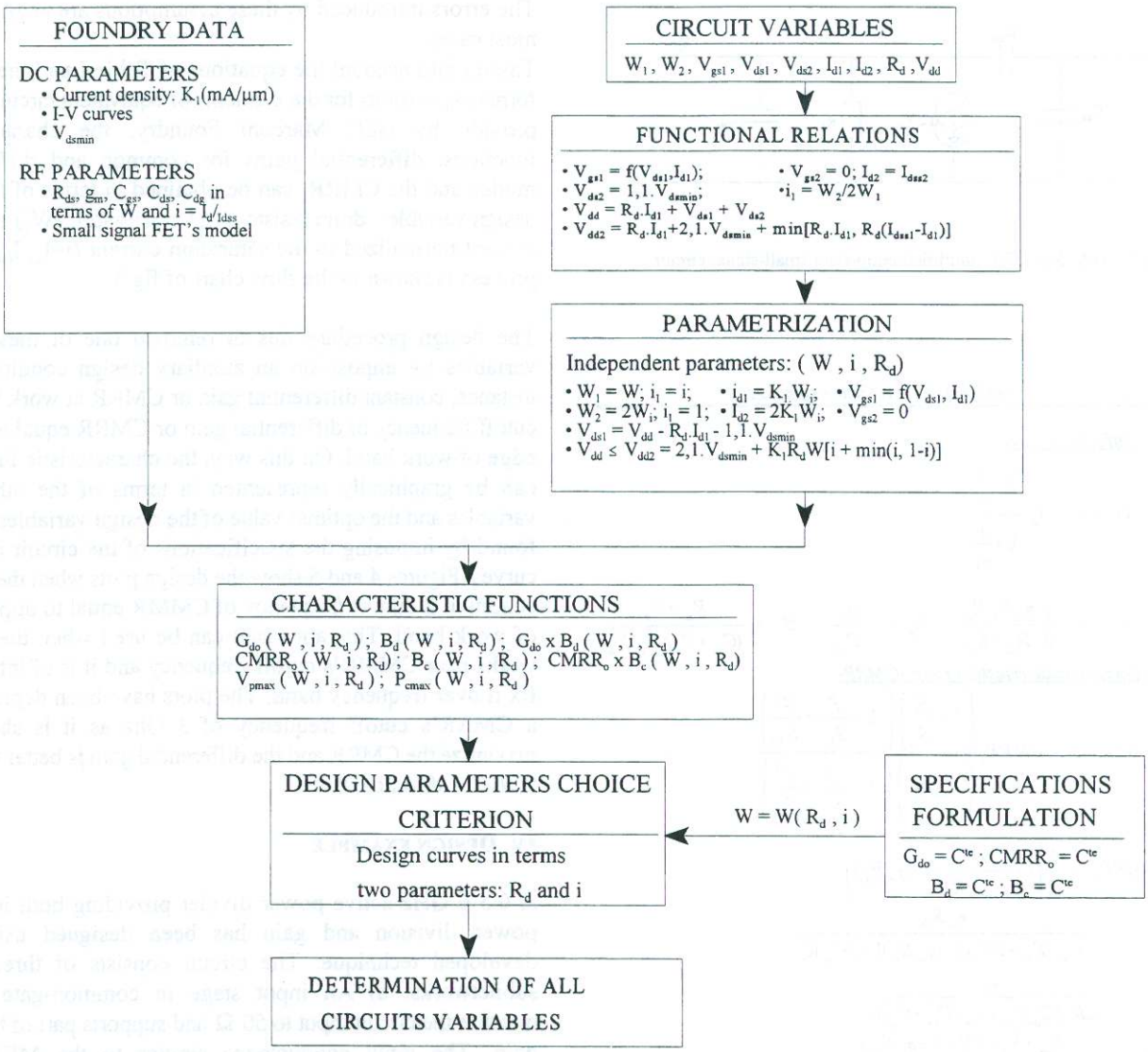

Fig. 3. Flow chart of the developed design technique

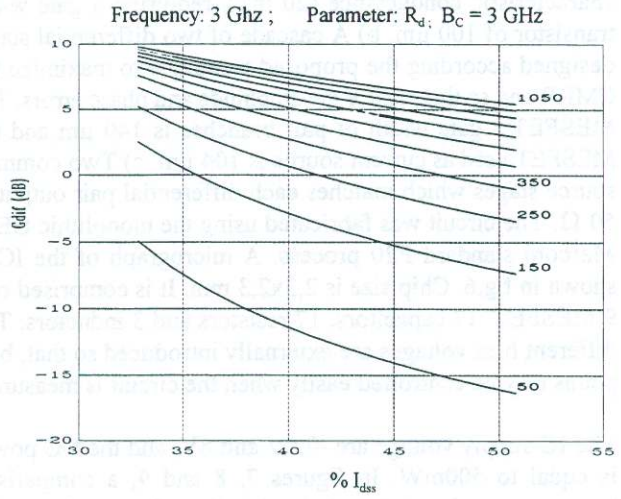

Fig.4. Differential gain with the "CMRRs cutoff frequency=3 Ghz" condition

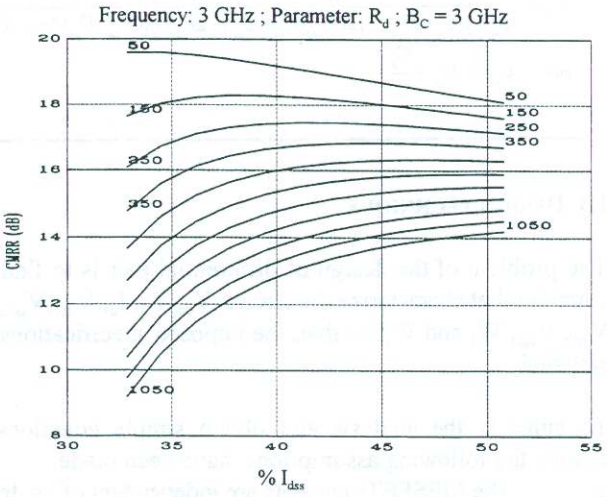

Fig.5. CMRR with the "CMRR's cutoff frequency=3 Ghz" condition

V. CONCLUSIONS

A design technique for GaAs differential amplifiers based on physical parameters of the GEC-Marconi foundry has been presented. A wide band power divider providing both in-phase power division and gain. An amplitude balance ≤0,2 dB and a phase balance ≤3° have been measured.

VI. ACKNOWLEDGMENT

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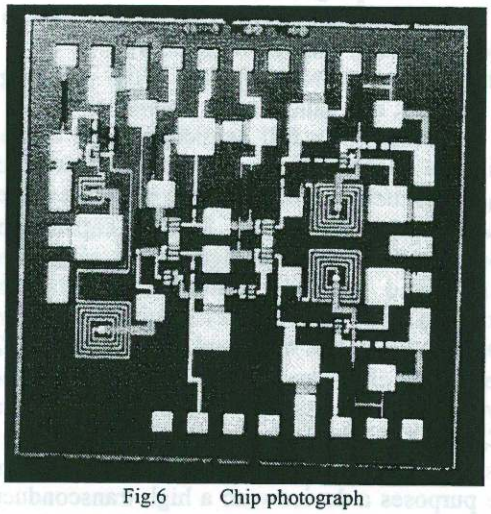

Fig.6 Chip photograph

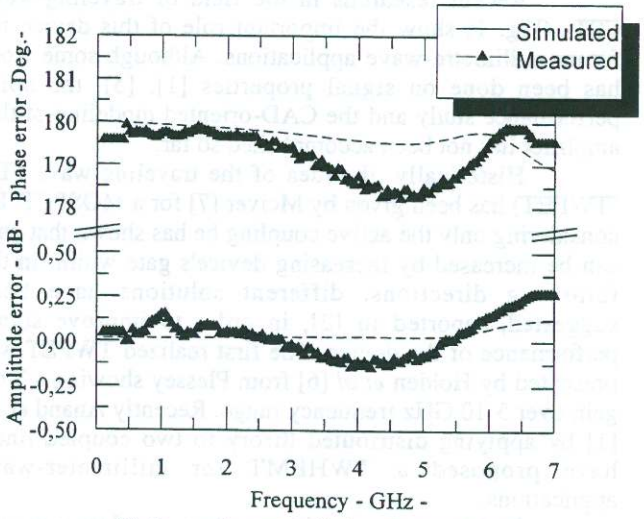

Fig.7 Output amplitude and phase errors

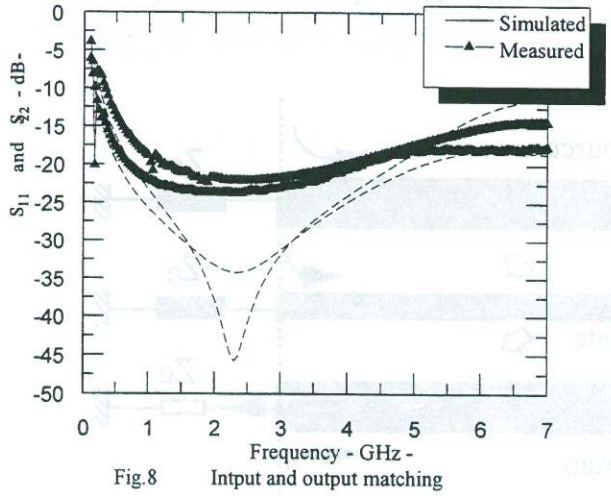

Fig.8 Intput and output matching

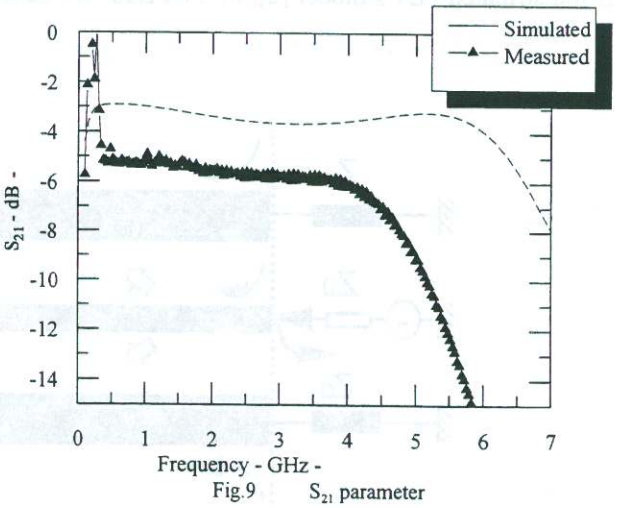

Fig.9 S_{21} parameter