Advantages of the New Generation Quasi-Monolithic Integration Technology (QMIT)

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Abstract: Fabrication process and advantages of the new generation quasi-monolithic integration technology are presented. The novel fabrication process gives excellent advantages such as extremely low thermal resistance, and a much lower thermal stress than the earlier QMIT concept [1]. This highly improves the packaging lifetime and electrical characteristics of the active devices. The fabrication process is simple and compatible with fabrication of high-Q passive elements. In comparison to the old concept of QMIT, elimination of air-bridges in this technology not only reduces the parasitics but also enables the fabrication of the rest of the circuit after measuring the microwave characteristics of the embedded active devices. This makes very accurate microwave and millimetrewave designs possible. Using the new fabrication process, microwave and millimetrewave circuits (with both coplanar and microstrip lines) containing power devices have for the first time been realised.

INTRODUCTION

To gain the advantages of silicon micromachining and III-V based active devices and to avoid the disadvantages of the standard hybrid and monolithic circuits, quasi-monolithic integration of III-V chips into silicon substrate is of utmost importance. The advantages, outlined in this paper, of the new generation QMIT over the earlier concept, considering the other common advantages of both technologies confirm it as an excellent alternative with unique advantages for microwave and millimetrewave monolithic integrated circuits.

THE NEW FABRICATION PROCESS

Two fabrication processes have been introduced, one for coplanar circuit realisation and one for microstrip circuit realisation. Steps 1a to 15a in Fig. 1 show the whole fabrication process for coplanar circuit realisation of the new generation QMIT and Steps 1b to 15b show the whole fabrication process for microstrip realisation. Details of the fabrication processes are given in [2]. Special attention has been paid to the gold electroplated layer (step 9b). A very thin layer of metal with a good adhesion should be deposited to prepare the substrate for electroplating. A thin layer of e-beam evaporated Ti (20 nm)/Pt (50 nm) which gives an excellent adhesion was used. This layer should cover the backside of the transistor and the holes completely. For this reason, the wafer is rotated around its axis and kept inclined to the direction of evaporation with a suitable angle during the metallization. Because of difference in thermal expansion coefficient of the thin layer metal and the positive photoresist, there are very narrow cracks, which separate the metal deposited on photoresist and the metal on the backside of the transistor and the silicon wafer. The cracks are very small and after some seconds of electroplating, the metal on the silicon wafer will be thicker and connects to the metal on the photoresist. The same happens for the metal on the photoresist and the metal on the transistor.

ADVANTAGES OF THE NEW GENERATION TECHNOLOGY

The earlier concept of QMIT was introduced to alleviate the problems of pure MMICs and of the conventional hybrid circuits. Although a few circuits containing low power active devices have been realised [1], the technology has suffered several shortcomings. The thermally conductive epoxy glue used to fix the GaAs-chips in the wet etched holes has a low glass temperature of 100 °C and a large expansion coefficient of 30e-6 1/K. The low glass temperature limits the working environment temperature to values well below the 100 °C and restricts the fabrication process to a very low temperature process. This renders the realisation of some passive elements such as MIM capacitors in this technology impossible. The large thermal expansion coefficient induces very high thermal stress, which significantly decreases the lifetime of packaging [3]. Considering the difficulties in removing the baked epoxy, cleaning it from the surface of the transistor or other parts was very difficult, if not impossible. Thermal conductivities of the available non-electrical conductive epoxies are not adequate for the power applications, so a very thick gold electroplated backside heat spreader was suggested [4]. On the other hand, defects occur during scribing of the chips by manufacturers. Some of these defects are in the form of protruding structures, which hinder the proper placement of the device in the etched holes. Proper realisation of the air-bridges requires the gap between GaAs-chips and silicon side-walls to 10

and 20 µm. Considering a common 5% tolerance in the thickness of the silicon wafers from the same company, having hole dimensions using a standard silicon wet etching with this accuracy is a hard task.

In the novel technology, active devices are fixed using low temperature plasma enhanced chemical vapour deposition (PECVD) amorphous silicon (for coplanar realisation) or an electroplated gold layer (for microstrip realisation). In this case the upper temperature limitation for the fabrication process is determined by the temperature specifications of the embedded chip itself, which should be well below 300 °C for the GaAs-chips. This is adequate for a successful realisation of the passive elements in this technology. The better geometrical construction and smaller deference in thermal expansion coefficients of the materials involved induce a much lower thermal stress distribution which results in a significant improvement of life-time of the packaging [5].

A thick layer of polyimide or other spin-on dielectrics gives a proper planarisation for the front-side metal deposition around the transistor. The air-bridges are not necessary anymore. The source terminal of the transistor is directly connected to the ground plane, this minimises the source inductance and improves microwave characteristics of the embedded transistor. Although a smaller dimension of passive elements is possible on a high resistivity silicon substrate than polyimide layer, by a suitably adjusting the dimensions of the coplanar waveguides and passive elements and the thickness of the spin-on dielectric layer, realization of the high-Q passive element is achievable. By elimination of the fragile air-bridges, the new fabrication process enables the fabrication of the rest of the circuit after measuring microwave parameters of the embedded transistor. This results in very accurate microwave and millimetrewave circuit designs.

At the end of the fabrication process the holes are either filled out with diamond-filled polyimide or a thick backside electroplated gold is used, which provides an excellent thermal resistance. Lower thermal resistance improves the lifetime of the packaging and electrical characteristics of the transistor.

MEASUREMENT RESULTS

DC characteristics of a Ka-band low-noise pHEMT in the coplanar line realization are shown in the Fig. 2. An 8 µm thick PECVD amorphous silicon layer fixes the transistor. On-wafer bias-dependent S-parameter measurements (0.1 - 40 GHz) for the same sample have been made using an HP 8510B network analyzer. Fig. 3 presents two sets of magnitude and phase plots of the measured S-parameters for the bias point of V_{gs} = 0.1 V and V_{ds} = 1.8 V. The measurements include the effect of coplanar line.

A good agreement between the measured DC and AC characteristics and the data given in the manufacturers data sheet was found. The current gain is smaller and the S21 is bigger than those of for the particular case given in the manufactures data sheet. This can be explained by the direct connection between the source terminal and the ground plane as compared to the four 200 µm long and 17 µm diameter gold wire-bonding in the manufacturers measurements.

CONCLUSION

A successful approach for integrating of the III-V semiconductor compound based active devices into the silicon substrate has been presented. The advantages are described and two fabrication processes for coplanar and microstrip realisations in this novel technology are introduced. In addition to great improvement of lifetime and thermal resistance of the packaging in comparison to the earlier concept, for the first time integration of the power active devices and high-Q low loss passive component fabrication have been possible.

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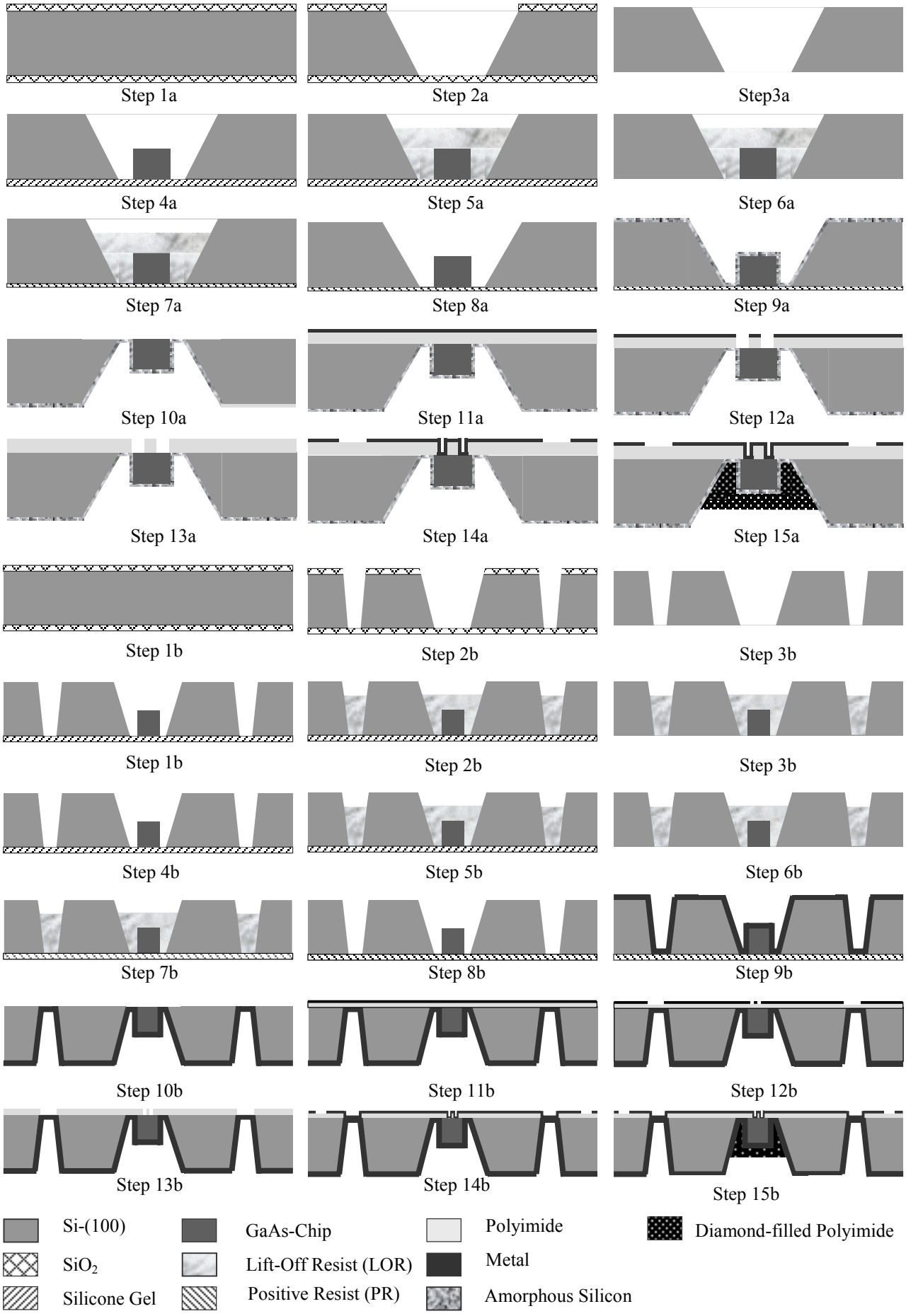

Figure 1: *Fabrication process steps for the coplanar and microstrip line realizations. Step 1a to step 15a illustrate fabrication process for the coplanar line realization and step 1b to step 15b illustrate fabrication process for the microstrip line realization.*

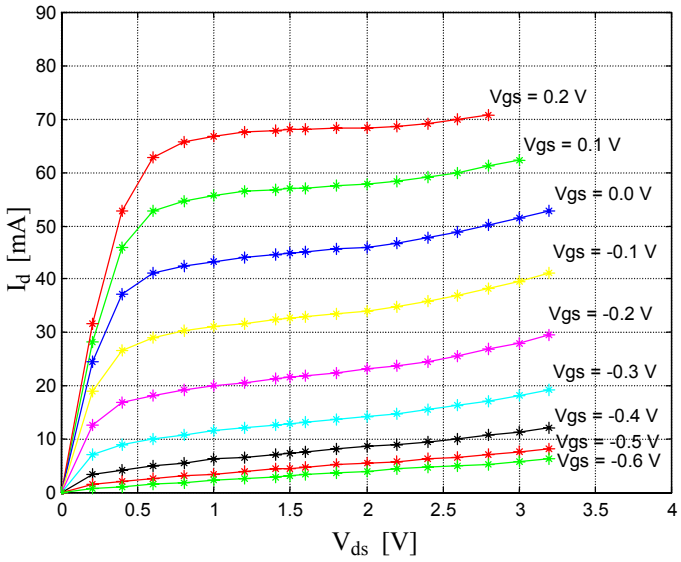

Figure 2: *I-V curves of the Ka-band low noise pHEMT with coplanar realization in the new generation QMIT. The transistor is only fixed by an 8 mμ thick amorphous silicon layer.*

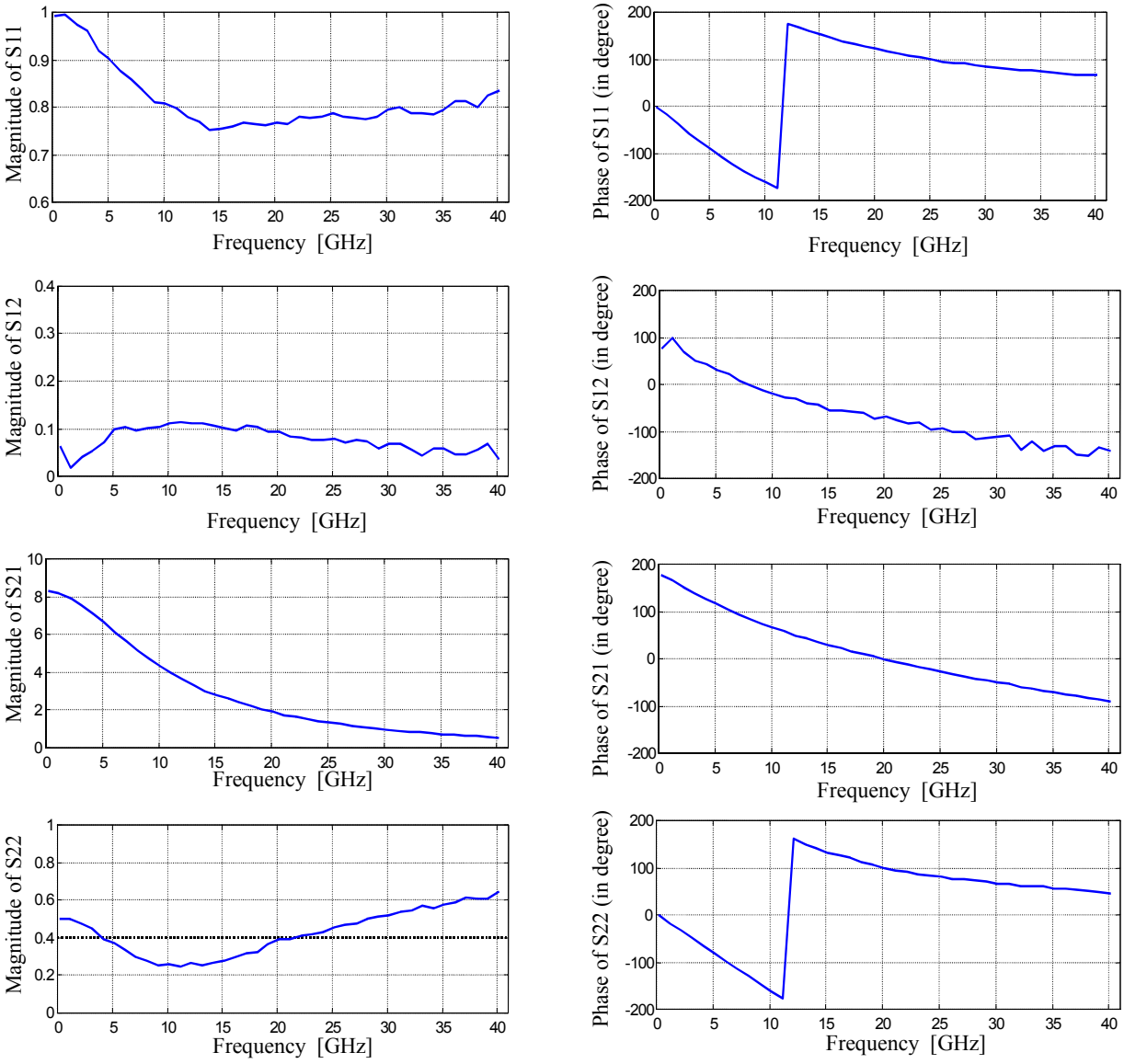

Figure 3: *S-parameter magnitude and phase plots of the Ka-band low noise pHEMT with coplanar realization in the new generation QMIT with bias point of V_{gs} = 0.1V and V_{ds} = 1.8 V.*