SiGe versus GaAs – is there a challenge?

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Abstract

There has been considerable recent activity with SiGe technology and much speculation that it will soon displace GaAs. Advances in conventional CMOS, over the years, have been based around device scaling. As submicron dimensions have been approached, further scaling of CMOS becomes increasingly complex and fundamental limits will soon emerge. The significance of SiGe is that it is compatible with conventional silicon processing and offers improved material properties, so that continued advancement can be sustained. We examine the present status of SiGe with respect to GaAs.

Introduction

The **GAAS 96** symposium is significant in that 1996 marks the 70th anniversary of gallium arsenide, that was first produced in 1926. It is also fitting that this symposium is held in the historical centre of Paris, as the element Gallium was a French discovery made over 120 years ago. Therefore it is appropriate to take this opportunity to review a little of the history of GaAs, to guage its level of maturity with respect to new materials such as SiGe. In a time when many new materials come and go, the historical maturity, device properties and intrinsic simplicity of GaAs ICs have caused a steady growth in the GaAs technology. Large volume applications are now a reality and, for instance, >90% of mobile phones now contain GaAs front ends. We discuss how this GaAs niche is expected to expand as the mobile phone concept shifts towards the interactive mobile multimedia personal communicator IM^{3}PC paradigm and we contrast this with the present status of SiGe technology. With SiGe we find that there appears to be only a HBT technology available, an increase in complexity and poorer substrate characteristics for high speed interconnects.

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GaAs Background

A. Gallium

On the 27th of August 1875, between 3 and 4 am in the morning (!), a French chemist by the name of Paul Émile Lecoq de Boisbaudran (1838-1912) discovered gallium by isolating it from zinc blende ore found in the Pyrenees. With a spectroscopic analysis he confirmed that he indeed had a new element and Lecoq identified this with Mendeleyev's prediction of the existence of 'eka-aluminium.' [1] There is some debate as to where the name 'gallium' comes from. According to some authorities it derives from the Latin *Gallia* meaning Gaul (France) and hence Lecoq named it in honour of his country. Other sources claim that it derives from the Latin *gallus* meaning a 'cock' and hence was named after Lecoq himself. [2]

B. Arsenic

Arsenic compounds have a long history going back into antiquity. The pure metallic form of arsenic (As) is called 'grey arsenic' and comes in the form of a flaky grey brittle metalloid. The name 'arsenic' was thought to come from the Greek $\alpha\rho\sigma\varepsilon\nu\iota\kappa\sigma\varsigma$ meaning 'male' – as the Greeks believed metals had different sex. However, the latest authorities now say it comes from the Arabic *az-zarnīk* meaning 'orpiment' – a compound of arsenic used as a yellow/gold pigment. In turn, *az-zarnīk* comes from the Persian word *zar*, meaning 'gold.' The first documented description of orpiment and realgar is due to Aristotle (384-323 BC). A neoplatonist by the name of Olympiodorus of Alexandria (*fl. ante* 550 AD) was the first to document white arsenic. The German alchemist and Dominican philosopher Albertus Magnus (*c.* 1206-1280) was the first to actually document metallic arsenic and its discovery is usually attributed to him.

C. Gallium Arsenide

Gallium Arsenide was first grown and chemically characterised in 1926 by Victor Moritz Goldschmidt (b. 1888, Zurich, d. 1947, Oslo). However it was not until the

[1] *Eka* is Sanskrit for 'one.'

[2] The authors guess that Lecoq made a deliberate *double entendre*!

early 1960s that researchers first attempted to make devices with GaAs. In 1965 Carver Mead produced the first GaAs FET. The GaAs FET began to find its first applications in the microwave area. The 1970s saw the first small scale integrated circuits but reliability was poor. The 1980s produced accessible and reliable GaAs foundries enabling realisation of large scale integration. By the late 1980s the scale of integration was sufficient for the contemplation of complex digital processing in GaAs. The early 1990s saw the first true VLSI GaAs designs. The present day quality and performance of GaAs has largely displaced the preconceptions about GaAs reliability, though some stigma from the 1970s still remains. Today applications abound and we see GaAs in >90% of all mobile phones, in satellite communication systems, optical fibre transceivers, ATM switching in telecommunication systems and high speed digital signal processing, to name a few. The main area where there has been a weakness is the GaAs CPU – research programs in this area lead by SUN and CRAY, for example, have all collapsed. The key problem is the gate leakage current in the MESFET, making large CPU memory in GaAs difficult to realise. This will now change as the complementary GaAs technology, using low leakage HIGFETs, has emerged [1]. The rate of growth in GaAs research has considerable momentum and this is illustrated in Fig. 1, which shows a remarkable increase in the number of GaAs publications. Whilst the number of publications is not an ideal measure of the health of the GaAs industry, it does reflect the increasing effort going into research.

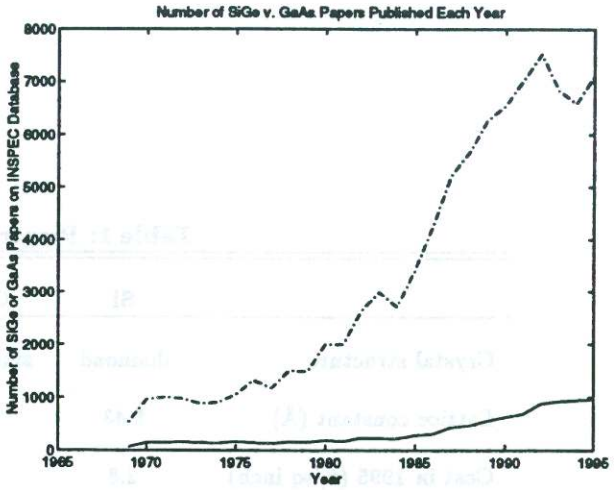

Figure 1: Number of published GaAs (chained line) and SiGe (solid line) papers on the INSPEC data base. The early SiGe papers were focussed on radiation detectors rather than heterostructure transistors.

Why SiGe?

Given that there are many alternative emergent technologies, other than SiGe, the question is 'why is SiGe selected as the main contender?' If we examine some of the main emergent technologies in Table 1 we see that in terms of cost and mobility, GaAs is clearly in the lead. SiGe becomes a closer competitor by virtue of the fact that costs are supposedly low, as it can be produced in existing silicon fabrication lines. Also SiGe attracts higher levels of R&D investment, as it rides on silicon funding sources. Unfortunately, it is difficult to enter a SiGe column in Table 1 – this is partly due to the fact that SiGe parameters will vary with mole fraction and particular heterostructure architecture, but is mainly because the open literature appears fairly silent for room temperature parameters. However, wherever sparse data is available, GaAs still remains superior. For instance, the effective electron mass of $Ge_{0.25}Si_{0.75}$=$0.264m_e$ [2] is 4 times heavier than in GaAs. Although, p-channel devices show higher mobility (around 1000 cm^2/Vs [3]), peak electron mobility in n-channel devices (3000 cm^2/Vs [3]) is still below that of GaAs.

SiGe Status

There are two kinds of SiGe starting material: **Type I** is a strained layer of SiGe on a silicon substrate and **Type II** is a strained layer of silicon on SiGe. As SiGe is a binary alloy, whereas III-V heterostructures employ ternary alloys, there is less control over tuning the lattice constant. [3] This, together with the 4% lattice mismatch between Si and Ge, means that SiGe is restricted to particular critical strained layer thicknesses depending on the mole fraction. It turns out for SiGe FET devices that the strained layer must be extremely thin (5-15 nm) and that it is susceptible to dislocations if processing temperatures go above 600 °C. The trend is towards lower fabrication temperatures, but at the present state-of-the-art this means that yield must be poor. Also limiting the thermal budget during processing often results in poorer oxide quality, incomplete dopant activation and poor passivation reflow resulting in reliability problems.

Carrier transport takes place at the Si/SiGe heterointerface, however as gate voltage is increased parasitic conduction at the Si/SiO_2 interface becomes a problem in MOS devices. Unfortunately, due to a fundamentally small conduction band offset in Type I devices, only p-channel MOS devices can be acheived. On the other hand, complementary MOS devices would be possible in Type II materials, however these suffer more from dislocations. There are no successful reports of fabrication of Type II MOS devices. Furthermore Type II is considered too complex for future mass production purposes [4].

[3] There have been recent attempts at attaining better control by adding carbon to obtain the SiGeC ternary combination. This may be successful, but work has only just started.

Table 1: Properties of emergent technologies.

	Si	GaAs	SiC-6H	SiC-4H	GaN	Diamond
Crystal structure	diamond	zincblende	wurtzite	wurtzite	cubic	diamond
Lattice constant (Å)	5.43	5.65	4.36	4.36	4.51	3.57
Cost in 1995 ($/sq inch)	2.8	21	2200	>2200	200	2000
Energy gap (eV)	1.12 Indirect	1.42 Direct	2.86 Indirect	3.2 Indirect	3.4 Direct	5.6 Indirect
Melting point (°C)	1412	1238	2800	2800	1500	4000
Thermal conductivity at 300 K ($Wcm^{-1}K^{-1}$)	1.31	0.46	4.3	4.3	1.3	20
Breakdown field (kV/cm)	300	400	>1000	>1000	3500	5000
Relative permittivity	11.9	13.1	9.7	9.7	8.9	5.5
Effective electron mass	$0.92m_e$ (longitudinal) $0.19m_e$ (tranverse)	$0.067m_e$	$1.5m_e$ (longitudinal) $0.25m_e$ (transverse)		$0.2m_e$	
Effective hole mass	$0.49m_e$ (heavy hole) $0.16m_e$ (light hole)	$0.50m_e$ (heavy hole) $0.076m_e$ (light hole)	$1.0m_e$		$0.8m_e$ (heavy hole)	
Refractive index	3.42	3.3	2.55		2.33	
Electron mobility at 300 K (cm^2/Vs)	1450	8500	500	1000	800	N/A
Hole mobility at 300 K (cm^2/Vs)	500	400	250	500	100(?)	500
Saturation velocity (cm/sec)	1×10^7	1×10^7	2×10^7	2×10^7	1.5×10^7	2×10^7

With Schottky gate devices, both Type I & II complementary devices are possible, however it turns out that the Schottky barrier height for the p-channel device is too low, resulting in high gate leakage current.

In summary, there are a number of unsolved problems preventing fully complementary digital SiGe technology. The technology is immature and it is suited to low temperature processing (600 °C max.) that has not arrived yet as state-of-the-art. To put the maturity of SiGe into perspective: the first SiGe FET was reported in 1985 [5], whereas the first GaAs FET was documented in 1966 [6] – hence SiGe has a maturity lag of upto about 20 years! By contrast, complementary GaAs has now been reported with VLSI packing densities [1] and densities of a million gates per chip are expected by the end of 1996.

Complementary MOS SiGe faces fundamental problems, however the complementary Schottky gate SiGe problem may be solved in the near future. In any case, the complementary GaAs (CGaAs™) HIGFET has emerged and has advantages over both MOS and Schottky SiGe. As the CGaAs™ HIGFET has a *semi-insulating* gate, it has a lower leakage current than Schottky SiGe devices and does not trap charge, as does the oxide in an MOS structure. Therefore the HIGFET has potentially greater tolerance to radiation and hot electrons than the SiGe MOS device.

Furthermore, SiGe cannot compete with the GaAs semi-insulating substrate for reducing parasitic capacitances. SiGe cannot presently compete with the OEIC capability of GaAs. Also the power added efficiency (PAE) and noise performance of microwave SiGe FETs cannot compete with GaAs. This means that GaAs is also the choice for mixed digital/RF mobile applications where compactness and hence a monolithic realisation becomes important, such as in the realisation of the single chip radio transceiver. Although it is often argued from an economics point of view that there is no market for the added expense of a such a single-chip solution, the shift towards the mobile multimedia paradigm will make strict demands on compactness and thus the the mixed digital/RF/optical capability of GaAs becomes even more attractive for future IM^{3}PC devices.

Another important factor with GaAs, that is often overlooked, is its inherent simplicity: no wells, no substrate ties, no latchup and over ten fewer masking layers than in BiCMOS. Conventional GaAs fabrication, such as through Vittesse, is now cheaper than BiCMOS. CGaAs also has over ten fewer masking layers than BiCMOS and a key feature is that n and p-channel devices differ by only two implant steps. GaAs also has a semi-insulating substrate, leading to low-loss high speed interconnects – proposals for a combined SiGe/SOI technology will have to deal with increased dislocation densities and all the attendant problems of SOI. In SOI, the film thickness is reduced, to combat the *floating body effect,* but this reduces the drain depth – giving rise to an increase in impact ionisation and hence reduced drain breakdown voltage. This places a premature limit on scaling, which defeats one of the main purposes of using SiGe. Holes from the impact ionisation also exacerbate the lateral bipolar snapback effect. Thin films on insulators also have thermal management problems, ESD protection problems and local heating effects that cause a drop in mobility, giving rise to negative slope resistance effects in the I-V characteristic.

Conclusion

SiGe HBT devices are the only SiGe devices showing signs of near-term success. However, GaAs MESFET power amplifiers show greater linearity and greater power added efficiency. The SiGe HBT is essentially a performance enhancement of existing bipolar technology with all its attendant strengths and weaknesses. Resistive substrates providing low-loss and high speed interconnects, such as in GaAs, can only be achieved by a SiGe/SOI combination which introduces many complexities. True VLSI digital circuits are not practical in an HBT technology due to lower packing density and higher power dissipation. Proposals to create a new BiCMOS comprising conventional CMOS with SiGe HBTs, will be faced with initially lower yields, greater complexity, greater number of masking layers and expense. As SiGe struggles to close the large gap in maturity against GaAs, facing all the economic and technical challenges described, GaAs in the meanwhile will have progressed further into the future.

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