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A constraint generation tool for the design of high frequency integrated circuits

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Abstract

Parasitic elements involuntarily introduced during the layout design play an important role in integrated circuits operating at very high frequency. Very often, in fact, the electrical performances of microwave networks strongly depend on the dimensions of parasitic elements, such as interconnection lines and net discontinuities. In this paper a new "constraint generation" CAD tool is presented. This program enables a quantitative analysis of the influence of parasitic dimensions on the final circuit performances and the singling out of most critical interconnections.

Introduction

In the design of an integrated circuit operating in the microwave frequency range, the physical layout drawings is a critical step, that is often manually performed by electrical designers. While in the digital field and in low-frequency analog applications the physical design can be often accomplished by CAD tools that automatically perform cell placement and interconnection routing, the layout design of a microwave network requires a detailed knowledge of the fabrication process technology and considerable insight into the electrical behavior of the network.

The main reason is the role played by the electrical parasitic elements involuntarily introduced during the layout design, that can significantly affect the electrical characteristics of the circuit under design.

In very high frequency applications, in order to prevent electrical performance degradation, the layout design is carried out by iterations of the procedure shown in fig. 1.

After the synthesis and optimization of the circuit, a first layout configuration is generated; thus, a new electrical netlist is generated, including most parasitic elements extracted by the physical representation of the circuit. The main parasitic elements are due to finite-length interconnections, line discontinuities and electromagnetic or thermal coupling effects between neighboring lines, active devices or passive lumped components. If the electrical characteristics exhibited by the circuit netlist including parasitics do not fit the specification tolerances, a new design cycle must be activated and a new layout is drawn. As an instance, in the design of a microwave amplifier, the electrical performances of interest can be the gain-bandwidth products, the output and input matching, and the phase margin.

This iterative, manual approach has several drawbacks.

- The manual design tends to be time consuming and error prone
- The extraction of parasitics is a rather a time consuming and cumbersome task
- If the parasitic extraction is accurate, the equivalent netlist can be complex and include a wide number of elements. If the electrical characteristic differ considerably from the expected values, no information is provided on the actual cause of performance degradation.

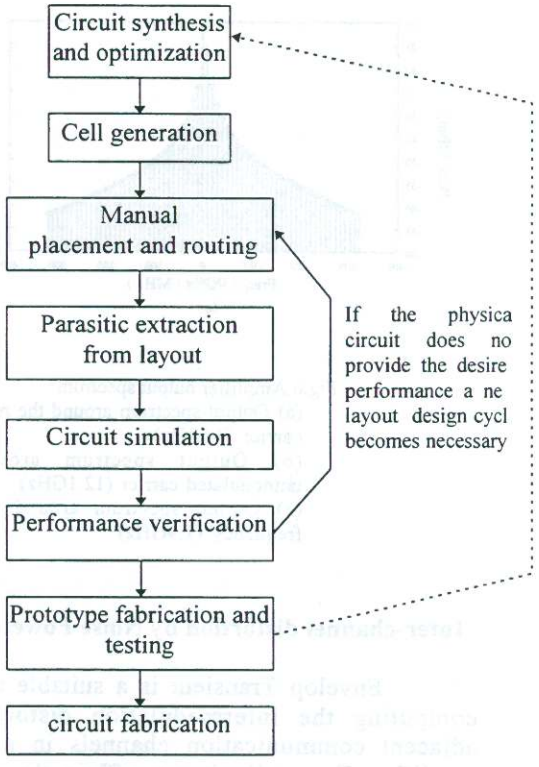

Fig. 1 Operation flow of the procedure employed in the manual design of analog circuits.

For these reasons, a different approach to the layout design of microwave networks should be pursued, taking also into account the increasing complexity of microwave systems integrated in monolithic or hybrid technology.

The tool presented in this paper is a fundamental block in a more complex system for the automatic and semi-automatic layout design of high frequency analog circuits, optimized with respect to the electrical performances. The tool has been implemented under the form of a CAD program, PickWick, which carries out the constraint generation task. PickWick analyzes the dependence of the electrical performances of an integrated circuit on the dimensions of parasitics introduced in the layout design, producing constraints on the parasitic dimensions that must be satisfied in order to preserve the circuit performances.

The paper is structured as follows. After a short review of the constraint generation problem, a short discussion is provided on the PickWick program; finally, the last section reports some numerical results and a discussion.

The constraint generation problem

In the physical design of microwave networks, general goals such as the total chip area and the overall interconnection minimization become of second order importance when compared to the target electrical performances. Several authors have pointed out that in the design of analog circuits that can be strongly affected by parasitic elements included in the layout, a constraint-driven approach should be preferred, [1,2]. In this approach, the cell placement and interconnection routing are performed by CAD programs that can handle both technological design rules and electrical constraints, i.e. boundaries on the maximum allowed dimensions of parasitic elements that must be respected in order to prevent significant degradation of the electrical characteristics of the final network.

The layout design of an integrated circuit in the presence of tight technological design rules and of requirements on the final electrical constraints, is a complex problem from the numerical point of view, [3], even for applications requiring a very low integration level, as in very high frequency applications. In the last few years several CAD tools for the automatic constraint driven layout design of analog circuits have been presented. These programs [4,5] perform the cell placement and the interconnection routing of networks even in presence of complex requirements, handling symmetric structures, satisfying demands on device matching by device merging and minimizing most critical interconnections.

Whether these tools could be successfully exploited in the layout design of microwave circuits is still an open question, since no CAD tool is up to now commercially available for the automatic physical design of high frequency networks.

On the other hand, while very little has been published in the literature on the constraint generation problem for analog circuits, [6,7], hardly anything has appeared on this subject purposely devoted to high frequency applications.

In the design of the constraint generation tool presented in this paper, the following assumptions were made.

1. In a microwave circuit, each electrical performance differently depends on the dimensions of each parasitic element. This dependence is neither linear nor monotonous.
2. The influence of the parasitic element dimensions on the electrical characteristics of a network, depends on the operating frequency.
3. The effects of different parasitic elements on an electrical parameter of the circuit, can reciprocally compensate.

Starting from these assumption, the program PickWick was designed to operate *a priori*, i.e. before the layout design, just after the circuit synthesis, to perform the following functions:

- analysis of the influence of the dimensions (length) of each interconnection line on the main electrical parameter of interest, in the whole operating frequency range;
- analysis of the influence of the dimensions of line-to-line coupling effects on the main electrical performances;
- approximated evaluation of compensation phenomena between different parasitics;
- classification of interconnections with respect to the different influence exhibited on the electrical parameter of interest.

Information provided by the constraint generation analysis can be employed for different aims, such as:

- verification of the robustness of a circuit topology, with respect to the introduction of parasitic elements;
- determination of the most suitable fabrication process technology, based on quantitative criteria. Very often, in fact, the choice between hybrid and monolithic technologies is determined by the role played by parasitic elements on the final performances of the network;
- constraints on the maximum (and some times minimum) dimensions that parasitics can assume, to be respected during the manual or the automatic constraint driven layout design.

The constraint generation program

The accurate and detailed investigation of the influence of the dimensions of all the parasitic elements that could possibly be inserted in the layout of an integrated circuit generates a complex problem from the algorithm point of view. In fact, in a network including λ electrical components, the number of interconnections will be at least of the order of λ, while the number of parasitic coupling elements will be of the order of λ^2 if only pairs of coupling nets are considered, and of the

order of λ^3 if also three-element coupling effects are considered.

Each electrical parameter Π of interest in a circuit is a function of Δ different parameters, where $\Delta=\lambda+\lambda^2+..+1$, i.e. each electrical parameter of the network is a nonlinear nonmonotonous function of a parameter set including the dimensions of the parasitic elements considered in the analysis and the operating frequency. In other words, $\Pi=\Pi(l_1, l_2,.... l_\Delta, \omega)$, where l_i is the dimension of the i.th parasitic element and ω is the circuit operating angular frequency. The analytical form of this functions is not known, but its numerical value can be sampled pointwise, each point requiring a circuit simulation. The maximum dimensions of the interconnections producing parasitics can be often estimated by information on the technological fabrication process, and the cumulative influence of all the possible parasitics could be in principle investigated by intensive use of circuit simulations. On the other hand, massive sampling of the functions relating the electrical performances of a network to the dimensions of the parasitic elements, would produce a huge amount of information, that would not always be easy to handle. For these reasons the first implementation of the program PickWick is necessarily based on some approximation simplifying the numerical complexity of the problem. In fig. 2 a scheme of the program PickWick is reported.

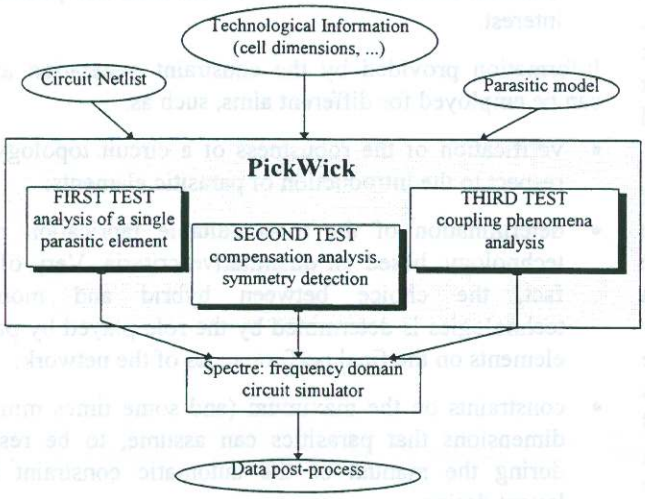

Fig.2 The structure of the program PickWick

The program PickWick takes as an input, a device level circuit description, some technological information to allow an approximated evaluation of the maximum dimensions assumable by the parasitic elements, and one or more electrical models that will be employed to reproduce the electrical behavior of parasitic elements during circuit simulations. In most cases, parasitics due to interconnections are efficiently modeled in terms of distributed microstrip lines; anyway, different models can be defined by the user based on other analytical models, on electromagnetic simulations or on experimental characterization of purposely designed test patterns. The program presents three different options. The first one automatically performs the systematic analysis of the dependence of the dimensions of each single parasitic on each single parameter of interest in the operating frequency range. Compensation effects between different parasitic elements are investigated in the second option, while in the third one, line to line coupling phenomena are evaluated. This partitioning of the problem allows a significant simplification of the constraint generation problem and provides an interactive simulation environment where a designer can drive the constraint generation process, by requiring a deeper investigation only concerning the parasitic elements that mostly affect the final circuit performances. PickWick is based on a circuit simulation program named Spectre, [8] that performs the steady state analysis of linear and nonlinear circuits in the frequency domain, by the harmonic balance method. The procedure adopted in PickWick is completely general and it does not depend on the particular circuit simulation tool adopted; nevertheless frequency domain circuit analysis was preferred since it is often employed in the design of high frequency integrated circuits.

Data produced by circuit simulations are sorted both in numerical and graphical form. A data post processor provides a hierarchical ordering of all the parasitic elements accounted for, based on the different influence exerted by the interconnections on the main electrical parameter of interest. If tolerance values are specified for each performance, the data post processor provides a variability range for each parasitic, in order to avoid electrical constraint violation

Results and discussion

In fig. 3 the schematic representation of a microwave amplifier, operating in the 4-8 Ghz range, is reported.

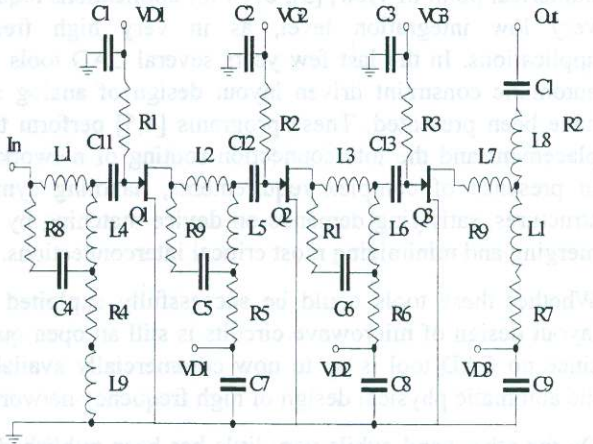

Fig.3 A microwave amplifier opearating in the 4-8 Ghz range

In fig. 4 and fig. 5 some data obtained using the program PickWick are reported. Fig. 4 reproduces the dependence of

the s-parameter S21 for the network of fig. 3, as a function of the dimension of a microstrip line introduced at node *Q1-gnd* of the network, and of the operating frequency. From the analysis of this three dimensional picture it can be observed that the function relating the parameter S21 and the dimension of the examined parasitic line is strongly nonlinear and that depends on the frequency. In fig. 5 a net classification produced by the program post processor is reported. Higher criticality coefficients indicate a stronger influence on the electrical parameter of interest. It can be noted that interconnections can be classified from *critical* to *non-critical* with the respect to the criticality coefficients that significantly vary from node to node. This classification can be suitably employed during the circuit placement, since it indicates those lines that should be minimized in order to avoid a performance degradation, behind the tolerance values specified by the user.

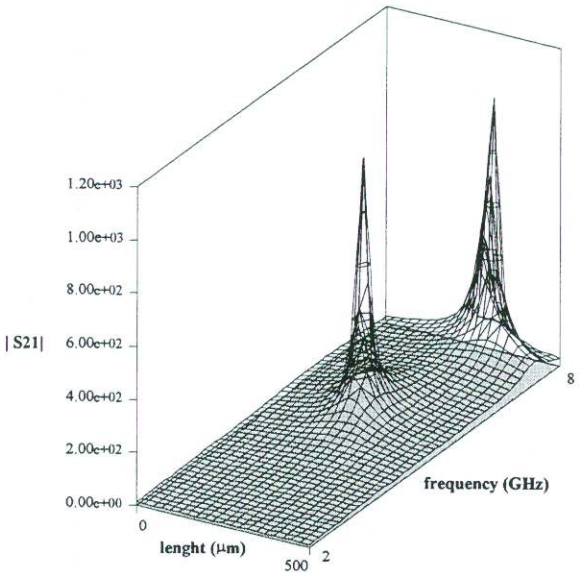

Fig.4 Module of S21 for the network of fig.3, vs. frequency and length of a parasitic line introduced in node Q1-gnd.

Conclusions and remarks

A new CAD program for the analysis of the influence of the dimensions of parasitic elements on the electrical characteristics of analog circuits operating at high frequencies has been presented.

This program is based on frequency domain circuit simulations and provides data that can be helpfully employed in the manual and constraint driven automatic layout design of microwave networks. Future developments will see the integration of the program PickWick, with Springs,[9] a new tool for the automatic constraint driven placement of analog circuits.

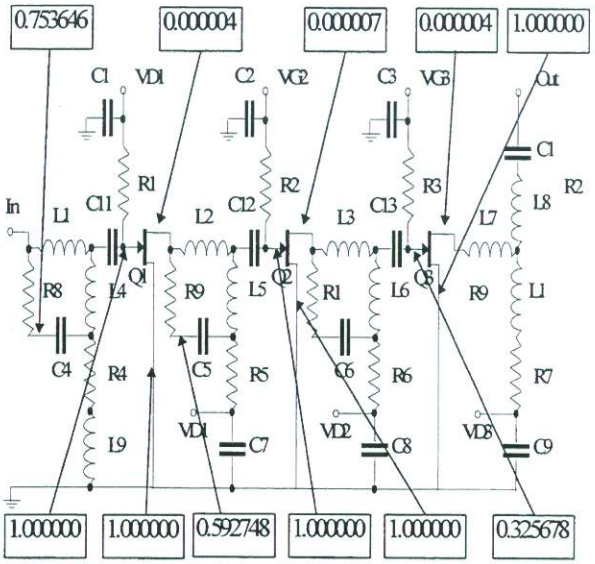

Fig. 5 Same examples of criticity coefficient (ranging from 0 to 1) which express the relative influence of parassitics on the electrical characteristic of the network. Value 1 represets the most influent interconnection.

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