Analytical Delay Model For Gallium Arsenide Digital Circuits

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Abstract

We present in this paper an analytical method for the evaluation of the performances of the BFL (Buffered FET Logic configuration) GaAs structures. Based on a representation of the average imbalance current, it allows direct evaluation of delays, with clear indication of technological, structural and environmental parameters, allowing the definition of sizing and optimization criteria. This method is validated through SPICE simulations on different configurations.

1. Introduction

Timing analysis is a very important tool for verifying the temporal correctness of digital circuits. It allows to compute path delays with an accuracy comparable to that of detailed circuit simulation but at a speed greater than that of logic simulation. Moreover clear knowledge of the contribution of technological and structural parameters to the individual delays allow direct definition of optimization rules for performance driven circuit design. If this approach is widely developed in Silicon technology to trade speed power and area on high complexity circuits [1, 2], few results related to III-V compounds are still available, they are mostly concerned with complex modeling of delays [3] or polynomial approaches [4] applied to DCFL family without detailed knowledge relative to the elementary design parameters.

We present in this paper a simple evaluation method of the performances of GaAs structures. Based on an explicit formulation it allows direct evaluation of delays, with clear indication of technological, structural and environmental parameters, allowing the definition of sizing and optimization criteria. This method is applied to the evaluation of BFL structures and validated through SPICE simulations on different configurations.

This paper is organized as follows. The delay modeling basically used for digital structures and its application to BFL structures will be given in the part 2. Explicit delay calculation will be detailed in the part 3. In part 4 we will present validation of these results through comparison with SPICE simulations. In the last we will draw a conclusion on the use and application of this explicit model in defining optimization criteria for performance driven design and dynamic test structures for process characterization.

2. Delay modeling

Accurate delay analysis must take into account real cell parameters such as technology, structure complexity, cell environment including total output load and input slope effects. We have already shown on CMOS structures [5] that, by using a physical modeling of the switching operation of the individual transistors constituting the gates under evaluation, it was possible to evaluate real propagation delays through explicit formulation taking full account of the input slope waveform, the output load and the structure size and configuration.

For that, dividing the data path into unidirectional elements, we obtained a real delay evaluation from a linear combination of the step responses of the driving (i-1) and the controlled (i) structures as:

\[ t_{HL\rightarrow LH}(i) = \frac{A \cdot t_{LH\rightarrow LH}(i-1) + t_{LH\rightarrow LH}(i)}{1 + A \cdot t_{LH\rightarrow LH}(i-1)} \]

where A, \( \alpha \) are defined in [5] and \( t_{LH\rightarrow LH} \) the fall and rise step responses of general AND/OR, evaluated for an output voltage variation from the static level to half the supply voltage.

These step responses have been obtained directly from the mean charge transfer evaluated across the node under consideration and produced by the imbalance current developed in the cell under evaluation as:

\[ \bar{I} \cdot \Delta t = C_{Load} \cdot \Delta V \]

where: \( \bar{I} \) represents the mean current imbalance across the structure under evaluation, \( \Delta t \) is the physical time under evaluation, \( C_{Load} \) the total output load and \( \Delta V \) the output swing. We propose to extend this work to BFL structures, with the objective to model the speed of these structures with sufficient accuracy through average evaluation of the charge transfer involved in the switching process.

2-a. Extension to BFL structures

The main difference between CMOS and BFL structures is in the ratioed operating mode of these structures in which the permanent current flow at low level modifies greatly the evaluation of the charge transfer. As shown in Figure 1, the BFL inverter is constituted of two parts: an inverter and a level shifter implemented both with depletion transistors. Pu and Pd transistors constitute the inverter, T2,
D1 and T1 implement the shifter. The voltage shift produced by the diode D1 biased through T1, insures level compatibility between input and output of the gates of this family. 

As a result we can consider the BFL basic cell, as constituted by an array of two independent parts: an inverter buffered by a level shifter.

![Digital inverter BFL diagram](image)

**Figure 1:** Digital inverter BFL.

As a consequence, the propagation delay of this BFL inverter will be considered as the sum of the delays of the inverter and of the shifter.

### 2-b. Active device modeling

As a first order attempt, the average current used in equation 2 is calculated from the JFET quadratic model derived from [6]. The main parameters involved in this model, threshold voltage and transconductance, are calibrated on the STATZ model [7] implemented in HSPICE [8], used as a reference simulator to validate the results obtained. Current equations involved are, in this modeling, given below:

\[ I = 0 \quad V_{gs} < V_t \]
\[ I = K \beta \frac{W}{L} \left(V_{gs} - V_t\right)^2 \cdot (1 + \lambda V_{ds}) \quad V_t < V_{gs} < V_{ds} \]
\[ I = K \beta \frac{W}{L} \left(V_{ds} - V_t\right) \cdot (1 + \lambda V_{gs}) \quad V_{ds} < V_{gs} - V_t \]

Where \( \beta \) represents the transconductance parameter, \( V_t \) is the threshold voltage, \( W \) and \( L \) are the real channel width and length, respectively, and \( \lambda \) stands for the output conductance. K parameter includes transconductance reduction induced by source access resistors, which have non negligible effects, for small values of the channel width. Typical parameters values extracted from the foundry model are: \( V_t = -0.985V \), \( \beta = 164 \cdot 10^{-4}/V \), \( \lambda = 0 \), \( K = 0.577 \) and \( L_{Max} = 0.8 \mu m \).

The channel charge modulation is modeled by two capacitances distributed between gate source and drain source. Their average contribution is evaluated from the static bias conditions through:

\[ C_{Moyen} = \frac{C\left( V_{gs\text{final}} - V_{gs\text{initial}}\right) + C\left( V_{ds\text{final}} - V_{ds\text{final}}\right)}{2} \]

### 3. Delay evaluation

Following equation 1, real delay evaluation is obtained from individual step responses, taking account of input slope effects. The evaluation of these step responses is detailed in the next part.

#### 3-a. Step response evaluation

Applying step control voltage to the input of the structures, produces instantaneous maximum current imbalance, resulting in minimum switching delay time. This value can be obtained easily from equation 2, evaluating the average current value from:

\[ I = \frac{\left( I_{ps} - I_{ns}\right)_{\text{initial}} + \left( I_{ps} - I_{ns}\right)_{\text{final}}}{2} \quad \text{For the inverter} \]
\[ I = \frac{\left( I_{ps} - I_{ns}\right)_{\text{initial}} + \left( I_{ps} - I_{ns}\right)_{\text{final}}}{2} \quad \text{For the level shifter} \]

and the output voltage excursion from:

\[ \Delta V = \frac{\left( V_{Out\text{final}} - V_{Out\text{initial}}\right)}{2} \]

where \( V_{Out} \) represents the output voltage of the structure under consideration and \( \frac{\left( V_{Out\text{final}} - V_{Out\text{initial}}\right)}{2} \) is the half logic excursion defined from the biasing conditions of the structure. Considering the switching delay time for the falling edge as an example, this results in:

\[ t_{\text{inv(lev)}} = \frac{C_{inv} \cdot V_{Out\text{final}} - V_{Out\text{initial}}}{K \beta \frac{W}{L} \left( V_{H\text{inv}} - V_t\right)^2 - \frac{1}{2} \frac{V_t^2}{\beta_{Conf}}} \]

for the inverter stage, and

\[ t_{\text{lev(lev)}} = \frac{C_{inv}}{K \beta \frac{W}{L}} \cdot \frac{V_{Out\text{final}} - V_{Out\text{initial}}}{2} \left( V_{H\text{inv}} - V_t\right)^2 - \frac{1}{2} \frac{V_t^2}{\beta_{Conf}} \]

for the level shifter, where \( \beta_{Conf} \) stands for the internal configuration ratio of the inverter, \( V_{H\text{inv}} \) is the input high level applied to the inverter, and \( V_{Out\text{final}} \) the resulting low input level controlling the shifter. Similar expressions are obtained for the rising edges of the two stages.

#### 3-b. Input slope effect

The propagation delay time given in equation 1 represents the difference of time occurrence of the input and output waveforms, evaluated at half logic excursion. The time spent by the input control voltage to reach the static logic level, represents a delay in setting the maximum imbalance current of the structure, resulting in an increase of the resulting switching delay.
This is illustrated in figure 2 where we have represented the evolution of the transient characteristics of the output voltage of the BFL inverter (HSPICE simulations), for different rise time values of the input voltage. As shown, output waveforms stay parallel, the effect of the input ramp is just a global translation of the waveform. This justifies the general equation given in part 2 (equation 1), in which the numerator expressed the propagation delay as a linear combination of input and output step responses. This is clearly shown in figure 2 (curves a and b) where the output is stable until the input reaches the maximum voltage. The denominator takes account of the necessary correction for slow input ramps: under these conditions the output varies under the imbalance current before the input reaches its steady state, resulting in a weaker contribution of the input ramp to the propagation delay.

![Figure 2: Output voltage of the inverter BFL for various rising input ramps (C_L = 200pF).](image)

\[ t_{\text{RLH/LH}}(i) = A \cdot t_{\text{RLH/LH}}(i-1) + t_{\text{HLH/LHH}}(i) - (i) \cdot D \cdot t_{\text{LHH/LHH}}(i-1) \]

with \( D = 2 \frac{V_{\text{ILH}} - V_{\text{in}}}{V_{\text{IH}} - V_{\text{in}}} \)

\( D \) is a non-symmetric transfer coefficient that we justify next.

As explained in the previous part, propagation delays are measured with respect to the half excision value of the respective voltages. Due to the specific biasing conditions of the BFL structures, static transfer characteristics suffer of large asymmetry, the values of the half excision voltages of the input and output do not correspond as illustrated on figure 4 where we give a realistic example of static transfer characteristic.

![Figure 4: Static transfer characteristic of the inverter BFL (\( \beta_{\text{diff}} = 5 \)).](image)

\( V_{\text{INT}}, V_{\text{IL}}, V_{\text{OLH}}, \) and \( V_{\text{ILH}} \) are the static logic levels, \( V_{\text{INH}} \) and \( V_{\text{OLM}} \) the value of the half excision of the input and output voltages, respectively. Let us call \( V_{\text{INH}} \) the value of the input voltage imposing the output voltage value at the half excision (\( V_{\text{OLM}} \)), as shown the difference (\( V_{\text{INH}} - V_{\text{INH}} \)) is significative and give indication of the lack of symmetry of the transfer characteristic. This difference induces an input slope extra delay represented by the \( D \) term, and which corresponds to the time spent by the input to vary from \( V_{\text{INH}} \) to \( V_{\text{INH}} \). Depending on the rising or falling character of the input slope, this correction term must be added or subtracted.

In the preceding equations, the \( (i-1) \) terms represent the time characteristics of the input control waveform, obtained directly from the linearized step responses of the corresponding stages.

### 4. Validations and results

In order to get a validation of the proposed analytic expression for real propagation times, we compare calculated and simulated values of the propagation delay times of an array constituted by two inverters (figure 5), and controlled by an input ramp of varying slope from 10ps to 500ps. Pull up and pull down transistor sizes are respectively chosen equal to 5\( \mu \)m and 25\( \mu \)m. Two diodes have been used for the level shifter, its transistor sizes have
been imposed at 10μm. This array, constituted by 4 logic stages, with each part loaded with 200fF, has been used as a demonstrator to validate the quality of the approximations involved in the preceding equation.

![Figure 5: Two cascaded inverters BFL have been used for the validation.](image)

Results obtained are given in Table 1. As shown, calculated and simulated values are in satisfactory agreement (less than 10% discrepancy between simulated and calculated values) and justify the approach we presented here.

### 5. Conclusion

Using a physical modeling of the switching operation at transistor level, through average parameters, we generalized, a previously defined explicit formulation of delays, to GaAs technologies with application to BFL structures. Delays are obtained as a combination of elementary step responses, with real account of structures, load conditions and input waveform effects. The accuracy of the resulting expressions has been validated through SPICE simulations.

As shown, for a given technology, real delays depend on the load, the size of the switching transistors and the size of the controlling device. It is then possible to use these expressions to define an optimization strategy for BFL structures, defining rules for transistor sizing under constraints. This is usually done from successive trial and simulations which are quickly limited to moderate complexity sets. Moreover, the clear evidence of technological and structural parameters gives the opportunity to define dynamic test structures [9] for the determination of average process parameters to be used for digital structures characterization. Under progress is the development of this formulation for DCFL structures.

### References


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Table 1: Comparison of calculated and simulated propagation delay times of 2 cascaded inverter BFL stages.