Multi-FET MMICs using GaAs MESFETs : Applications and New Developments

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Abstract

Multi-MESFET MMICs have a key role in high frequency communication systems for a variety of linear and nonlinear functions. Following a review of a systematic synthesis procedure and some example circuits already implemented, this paper addresses the key issue of distortion generation in multi-FET circuits and also the device models needed for understanding the distortion mechanisms and prediction of nonlinear circuit performance. Finally, some techniques for reducing the distortion generated are considered and applied to an isolator and a frequency doubler.

Introduction

Developments in personal, mobile and computer communications are creating a need for communication circuits in integrated circuit form with good performance and low cost. In order to minimise the cost of design, there must be good understanding of circuit capabilities in order to avoid the need for extensive optimisation in every case. In order to minimise the cost of use, performance of the chip itself in terms of distortion must be such that external filters and extensive tuning operations can be eliminated or at least minimised. In contrast to conventional MMIC designs in which the number of FETs is strictly minimised, multi-FET MMICs use structures such as cascodes and differential pairs to improve functionality and in an attempt to improve performance. However, in general, the effect of parasitic components is such as to lead to high distortion performance at microwave (and even at VHF) frequencies. It is clear that in order to realise the potential advantages of multi-FET MMICs and minimise costs of design and use, as we require, it is necessary to develop a profound understanding of circuit operation and performance. These in turn rely in good techniques for circuit simulation and device modelling.

After a review of a systematic synthesis procedure and some existing requirements which we have met, this paper will address the critical issues of the effect of device imperfections on circuit performance, device modelling and distortion compensation of MMICs, both by changes to FET gate widths and to circuit topology.

Review of Systematic Synthesis Technique

In [1], a systematic synthesis procedure is proposed for the realisation of both linear and non-linear circuit functions using depletion-mode FETs, assumed to be described by a square-law relationship between drain current I_d and gate-source voltage V_{gs}

$$I_d = \beta\left(V_{gs} - V_T\right)^2 \qquad (1)$$

The circuit architecture consists of two parts, namely an output stage and a voltage processing block. The output stage consists of m FETs with their sources connected to the output node (source FETs) and n FETs with their drains connected to the output node (sink FETs). The gate-source voltages of the source and sink FETs are defined as linear combinations using coefficients 1, -1 and 0 of the system input voltages. For this arrangement, the output current may be written

$$I = \beta\left[\mathbf{v}^t\left(\mathbf{A}^t\mathbf{A} - \mathbf{B}^t\mathbf{B}\right)\mathbf{v} + 2\mathbf{v}_T^t(\mathbf{B} - \mathbf{A})\mathbf{v}\right] \qquad (2)$$

where $\mathbf{v}$ is a column vector of system input voltages, $\mathbf{V_T}$ is a column vector of constants V_T, and $\mathbf{A}$ and $\mathbf{B}$ are matrices containing the coefficients for the source and sink FET gate-source voltages. Using (2), the coefficients $\mathbf{A}$ and $\mathbf{B}$ may be chosen to yield required circuit functions. The second term in (2) yields linear functions, such as selfconductances, transconductances, negative conductances, signal splitters and combiners, and the first term non-linear functions, such as multipliers and frequency doublers. Having determined the $\mathbf{A}$ and $\mathbf{B}$ coefficients required, the voltage processing block is designed to realise the source and sink FET gate-source voltages in terms of the system input voltages, using various building blocks. Basic lcircuit functions may be combined to realise higher level circuits and we now give a previously implemented example of an isolator realised using linearised self and trans-conductor circuits.

Review of Existing Implementations

A. Isolator [2,3]: The isolator is an important microwave component and is an ideal test vehicle for multi-FET MMICs. The isolator design in Fig 1a consists of a cascade of a linearised selfconductor, a linearised transconductor and another linearised selfconductor. Both the gain and the input and output resistances may be linearly electronically tuned. The circuit was fabricated using the GEC Marconi F20 GaAs MESFET process via EUROCHIP and the layout is shown in Fig 1b. The measured s-parameter performance (Fig 1d) is close to the required simulated performance (Fig 1c).

B. Active Resonator [4,5]: The integration of microwave subsystem components such as amplifiers and mixers is progressing rapidly but filters, which are essential system components, have proved more difficult to integrate. A potentially promising approach is to simulate inductors using active circuits which can allow tuning of centre frequency and Q-factor. Fig 2a shows the circuit diagram of a single active resonator consisting of a loop of a positive and a negative integrator, each realised as a transconductor with load capacitance. The circuit was fabricated with the GEC Marconi F20 process (Fig 2b) and the measured reflection coefficient, (Fig 2d) is close to the simulated curve in Fig 2c. Resonant frequency is 1.47 GHz. Built-in Q-factor tuning can give arbitrarily high Q-factor subject to post-tuning component variations. The closeness of measured and simulated performance establishes feasibility for use in high order filters.

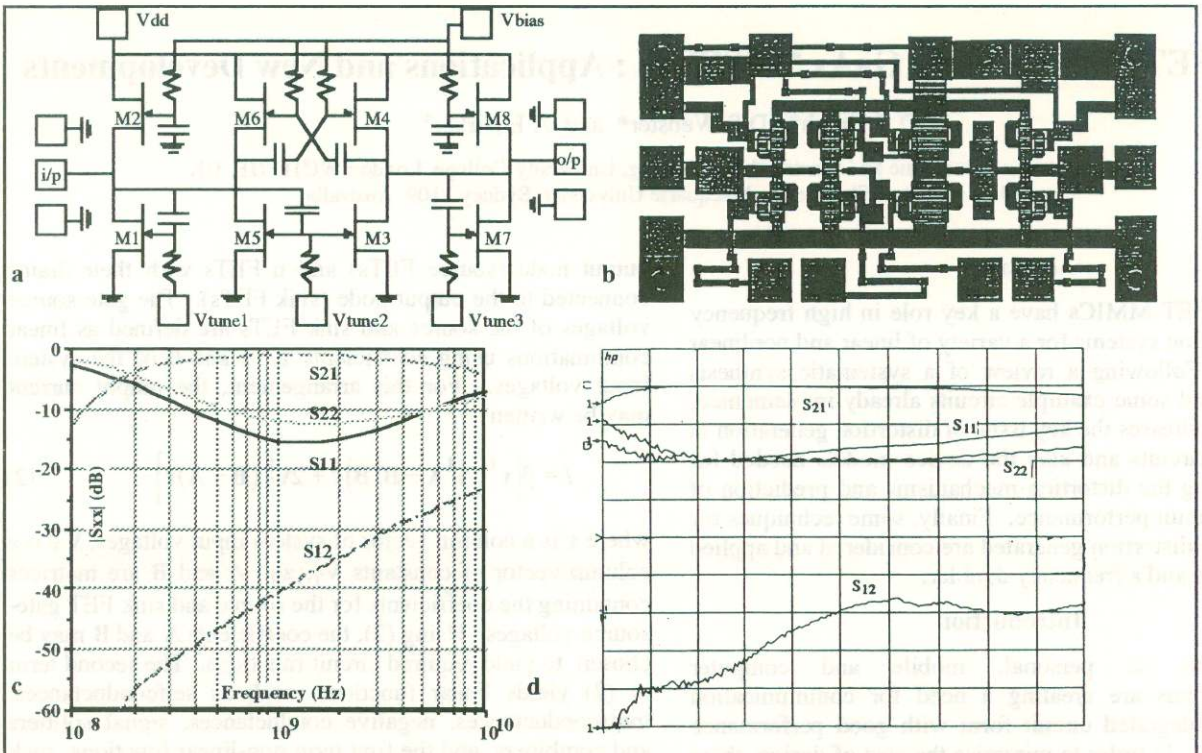

Fig 1 Isolator MMIC a Circuit diagram b Layout plot c Simulated s-parameters d Measured s-parameters (scale: 0.5 to 5.5 GHz; 5 to -45 dB)

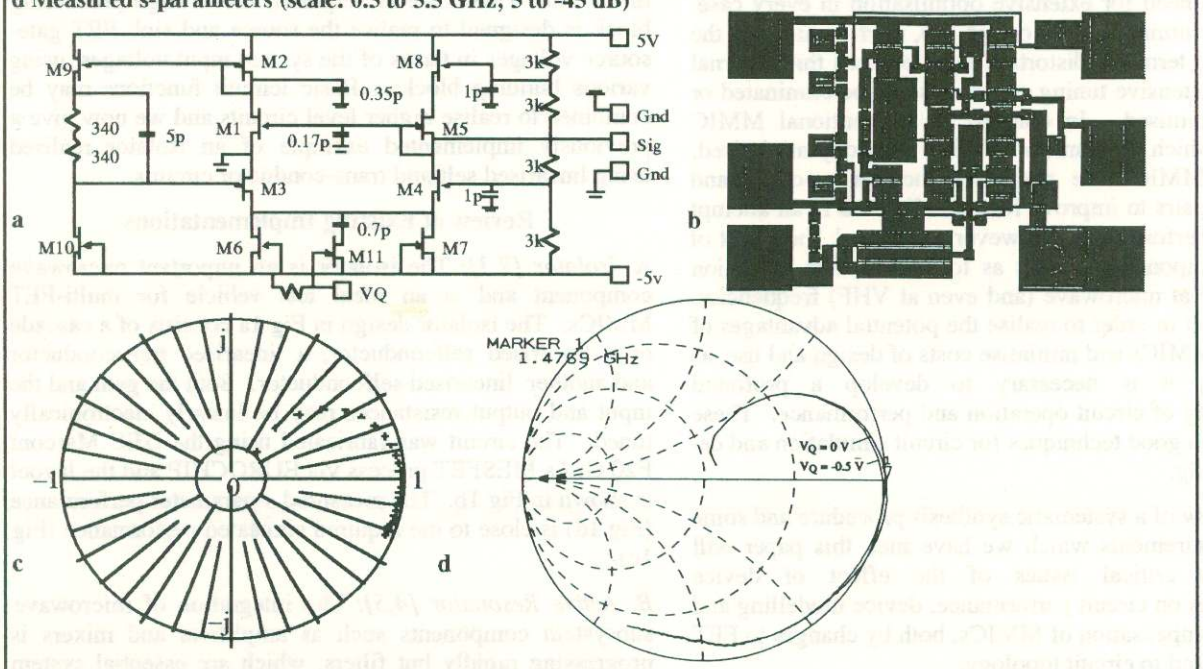

Fig 2 Active filter resonator a Circuit diagram b Layout plot c Simulated reflection coefficient d Measured reflection coefficient

Device-Circuit Interaction

The synthesis described above relies on the simple model of (1) which does not include finite and non-linear output conductance, parasitic capacitances (defining device bandwidth) and general power law behaviour. These factors will cause distortion, which has been found to increase with frequency and which limits circuit operating frequency to a small fraction of the small-signal bandwidth. Successful exploitation of high frequency multi-MESFET circuits relies on accurate analysis and compensation of this effect.

Our initial analysis is based on the simple model of Fig 3, which consists of a non-linear voltage-controlled current source representing the core of the device

$$I_d = g_0 + g_1 V_{gs} + g_2 V_{gs}^2 + g_3 V_{gs}^3 + \ldots \qquad (3)$$

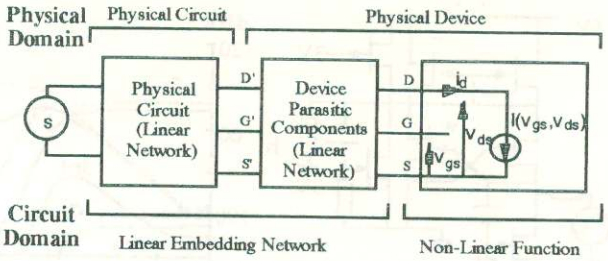

Fig 3 Non-linear device and linear embedding network

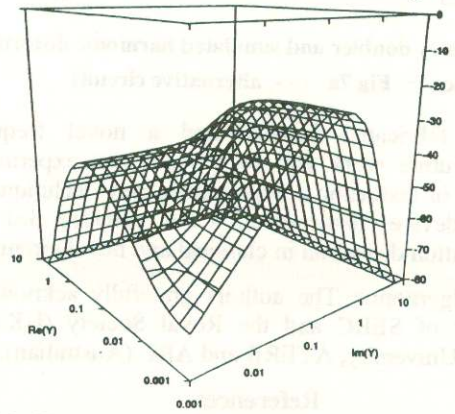

Fig 4 3rd harmonic in I_d versus Re [Y] and Im[Y]

and an embedding network comprising excitation, source and load impedances, feedback and bias elements elements and parasitic elements associated with the device. If the embedding network is assumed to be linear, it can be described by

$$I_d = AS + YV_{gs} \tag{4}$$

where S is the excitation, A an excitation constant and Y a constant referred to as the interaction admittance. It may be shown [3,6,7] that, for a wide range of practical circuits, Im[Y] is primarily dependent on device capacitances which determine the device bandwidth or f_T and that Re[Y] describes loading and feedback effects. Interaction between (3) and (4) leads to a pattern of distortion harmonic components in device I_d and V_{gs} [3]. In general, all harmonic components tend to increase proportionally to both Im[Y] and Re[Y] reaching a peak before falling off with a gradient which increases with harmonic order. The peak occurs for a value of Im[Y} which corresponds to a frequency just below the device f_T. Fig 4 shows a typical result for the 3rd harmonic distortion in the current of a common-gate FET. The theory has been used to attribute 3rd order distortion in the common-source amplifier to the interaction of 2nd order transconductance non-linearity (g_2 in (3)), with linear parasitic c_{gs} [3] and r_S [6,7]. The behaviour of rising distortion with frequency imposes a fundamental limitation on all analog circuits, from simple ones with a single device to complex circuits as in Fig 2. The compensation of distortion caused by device-circuit interaction will be considered in a later section.

GaAs MESFET Modelling

Accurate modelling and characterisation of devices is critical to successful circuit design and simulation, especially for intermodualion distortion specifications. Our work has adopted the Parker-Skellern MESFET model [8],

Table 1 Features of the Parker Skellern model

(1) Independent **Non-square law** behaviour of Non-saturated and Saturated regions.
(2) Frequency Dependant **Electrostatic Feedback**
(3) Low Frequency **Channel Heating**
(4) **Subthreshold** Intermodulation Minimum
(5) Parameters to **shape Triode-Saturation Transition** region.
(6) Improved version of **Statz Non-linear Capacitance** equations.
(7) Extrinsic **Resistances**.
(8) Gate-Source and Gate-Drain **Leakage and Breakdown** currents

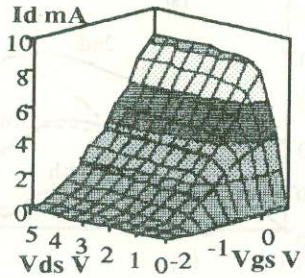

Fig 5 Typical pulsed I-V MESFET characteristic

which has the unique combination of features in Table 1 and runs on SPICE3 [9]. Pulsed characterisatiuon leads to I-V characteristics, as in Fig 5, eliminating low frequency anomalies due to trapping, history and rate dependence and thermal effects [10].

Understanding of circuit distortion generating mechanisms, in which device-circuit interaction [3] plays a critical role, is facilitated by developing intermiediate level models which approximate the Parker-Skellern model but which are amenable to hand analysis. The complex dependence of device I_d on V_{gs} and V_{ds} can be represented at a given operating point by a 2-D Taylor series

$$i_d = g_0 + g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + .. g_{ds1} v_{ds} + g_{ds2} v_{ds}^2 + g_{ds3} v_{ds}^3 + .. m_{11} v_{ds} v_{gs} + m_{12} v_{ds} v_{gs}^2 + m_{21} v_{ds}^2 v_{gs} + .. \tag{5}$$

The coefficients of (5) can be determined from device pulse measurement data by numerical techniques and they relate directly to distortion generation mechanisms in circuits. Thus, they allow us to assess the accuracy of models in a realistic way and are being used to devlop distortion compensation techniques in multi-FET circuits. These coefficients provide an invaluable direct link between device measurement data and complex circuit distortion performance. Study of the device representation of (5) in the context of device-circuit interaction theory is leading to the possibility of designing practical circuits to meet given distortion specifications.

Distortion Compensation

A General: Application of device-circuit interaction theory with appropriate MESFET models shows that most multi-MESFET circuits suffer from severe generation of unwanted distortion components, particularly at high frequencies. However, the systematic approach to modelling and analysis developed can lead to methods of compensation for distortion. An attractive idea, still in its infancy, is to eliminate or reduce the device circuit interaction effect at source

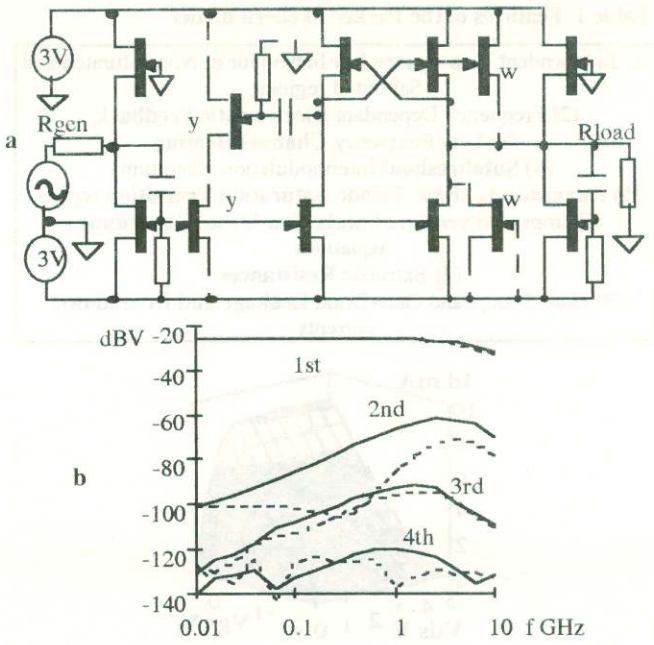

Fig 6 Compensated isolator and simulated distortion characteristic (— unoptimised - - - optimised

by modifying the circuit to cancel the YVgs term in (4), which describes the device embedding. This can be accomplished by the addition of a 'dummy' device at 'critical' nodes [3]. Another technique is to correct for signal unbalance in a push-pull output stage by scaling the output device gate widths and by the addition of phase correcting resistors [11,12]. We briefly give two examples.

B Isolator: Fig 6a shows the compensated version of the isolator of Fig 1a in which FETs *w* balance the output stage (1) and FETs *y* are to reduce device circuit interaction [11]. The dashed curves in Fig 6b show the improvement in distortion obtained considerably extending the useful bandwidth of the circuit.

C Frequency Doubler: Fig 7a shows a frequency doubler developed using the general synthesis described above. The circuit has the interesting property that it does not possess a 'critical' node where device circuit interaction takes place. The simulated curves in Fig 7b show the much reduced level of 3rd harmonic at high frequencies for this circuit compared with that for a similar circuit which does possess such a critical node [11]. It may be shown that the primary mechanism for generation of 3rd harmonic is due to m_{11} and g_3 in the FET model (5) which give contributions of opposite polarity. By chosing the output FET gate-width correctly in relation to the load resistance, a null in 3rd harmonic can be produced leading to a high quality broadband response [11].

Conclusions

We have considered multi-FET MMICs. Review of an existing isolator and an active filter confirms feasibility as far as small signal performance is concerned and attention then focuses on device modelling and device circuit interaction concepts which are essential for achieving the low levels of intermodulation distortion required in practical applications. Distortion compensation is developed and applied to the

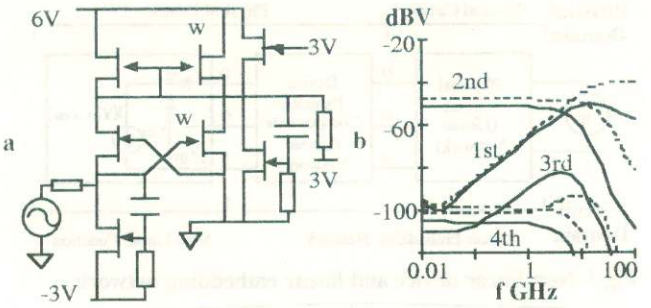

Fig 7 Frequency doubler and simulated harmonic distortion characteristic (— Fig 7a - - - alternative circuit)

previously fabricated isolator and a novel frequency doubler. Future work will be focussed on experimental verification of distortion compensation, new techniques for non-linear device characterisation and reducing 3rd order intermodulation distortion in classical and novel circuits.

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