Broadband frequency divider for mobile communications systems

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Abstract

Recently, a new configuration has been proposed for the design of MMIC frequency dividers [1]. Following this method, a MMIC broadband analog frequency divider in the millimetric range has been designed and manufactured for applications in mobile communication systems. Non-linear simulations of the device have been performed, showing the ability of H.B techniques to handle such complicated functions. Finally, comparisons between calculated and measured results have been performed, exhibiting a good agreement.

Introduction

The frequency division is a key function for an important number of microwave applications, such as phase-locked loops or frequency synthesizers. For high frequency operations, such as encountered in mobile communication systems, frequency dividers operating from millimetric frequency band have to be designed, both for receiver and transmitters functions. These dividers must be of analog type. Regenerative frequency dividers [2] can be used for that purpose but they often suffer from a limited frequency bandwidth. Thus there is a need for designing broadband analog frequency dividers operating from the millimetric waves region. Such dividers can be realized by phase-locking an oscillator with one of its harmonics. This supposes a highly non-linear operation of the device. Thus accurate non-linear simulation techniques [3] are required to validate the design process.

These techniques have been successfully applied to the design of a Ka Band divider operating over a 15% frequency bandwidth. A realization was made on a 0.25μm HEMT technology and a 26.8 to 31.2 GHz input bandwidth has been measured for 0dBm input power.

Design and simulation

The new broadband configuration [1], composed of two transistor stages (amplifying and regenerative), is shown in Fig.1. In order to obtain a broadband operation, an open loop optimization of the regenerative stage must be performed, imposing, in the operating band, a zero value and a minimum frequency variation of the phase difference ϕ, between the voltages, V_e and V_s, at the input and output of the feedback loop:

$$\frac{d\phi}{dw} \to 0 \qquad with \quad \phi = \angle \frac{V_s}{V_e} = 0$$

These two conditions ensure the phase locking of the circuit over a frequency band.

Two different broadband divider configurations are possible depending, respectively, on the series or parallel connection of the feedback network. The blocks diagram shown in Fig.1 corresponds to the second type.

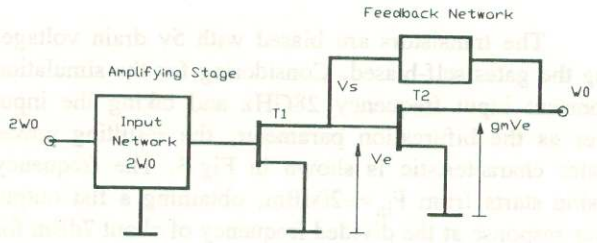

Fig.1 Broadband configuration

For the divider simulation, the harmonic balance technique has been used. The divider analysis method, based on the measuring probes technique [3], allows the simulation of the circuit as if it were a forced system, satisfying a condition of non-perturbation of the steady state. The divider bifurcation diagrams [3],[4] as a function of the two parameters of interest (the input generator power and frequency), provide a powerful method to determine the phase-locking bands. A local stability analysis, based on the Nyquist criterium [4], completes the simulation process, allowing to determine the stable branches of the solution paths.

Monolithic frequency divider

The above techniques have been applied to the design and simulation of a MMIC frequency divider by two

with 28GHz input frequency. The circuit schematic is shown in Fig.2. The substrate is GaAs with dielectric constant $\epsilon_r = 12.8$. Each transistor is composed of two parallel cells, being the total gate width 2x50μm for the first transistor and 2x75μm, for the second. The non-linear elements taken into account for the FET model are, in each case, the Schottky barrier current I_{gs}, the drain current I_{ds} and the input diode capacitance C_{gs}. For the inductors and capacitors in the linear part of the circuit, the MMIC models provided by the THOMSON foundry have been used.

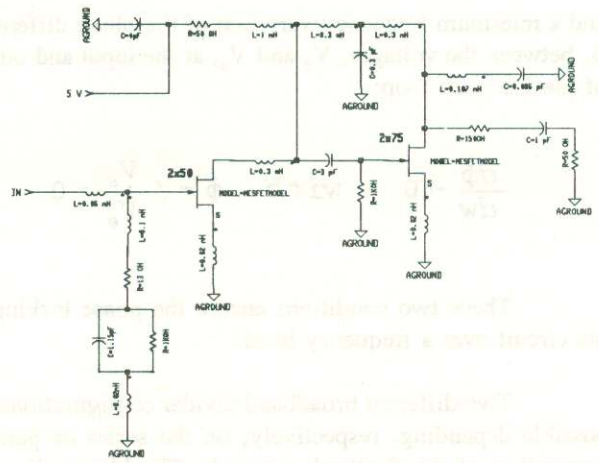

Fig.2 Circuit Schematic

The transistors are biased with 5v drain voltage, being the gates self-biased. Considering for the simulation a constant input frequency 28GHz and taking the input power as the bifurcation parameter, the resulting power transfer characteristic is shown in Fig.3. The frequency division starts from $P_{in} = -20$dBm, obtaining a flat output power response at the divided frequency of about 7dBm for most of the input range. A double solution, due to the presence of a turning point, can be observed. However, the stability analysis shows that only the upper solution branch is stable. Experimentally, the frequency division starts as well from very low input power at this frequency, obtaining also a flat output power response. This can be seen in Fig.4, where the experimental transfer power curves have also been traced for other input frequencies. All measurements have been performed on wafer.

In Fig.5 the circuit bifurcations diagrams as a function of the divided frequency have been traced for different input powers. In all cases flat output power response and broadband operation can be observed. As the input power increases, there is a reduction of the upper end in the divided frequency band, due to the appearance of an hysteresis phenomenon. This has also been experimentally observed, as shown in Fig.6, where the measured minimum and maximum frequencies in the synchronization band have been traced versus input power between -10 and 5 dBm. The resulting synchronization bandwidths correspond to about 15% of central frequency.

The output power measurement for $P_{in} = 0$dBm are shown in Fig.7. These measurements have been performed on wafer, obtaining the operation band 13.4-15.6 GHz. An output buffer amplifier allows to obtain a very flat output power of 8dBm. The good agreement between simulation and experimental measurements validates the new design and simulation techniques.

Conclusions

A new broadband configuration for regenerative dividers has been proposed, allowing broadband operation at the millimetric frequencies. The dividers are simulated through harmonic balance, combined with the measuring probes technique, which allows an accurate prediction of the circuit performance. These techniques have been applied to the design of a monolithic frequency divider in Ka Band, obtaining about 15% operation bandwidth and an excellent agreement between measurements and simulation.

Acknowledgements

This work was partially supported by the CEC under RACE II project n°R2067, "Mobile Broadband Systems".

References

[1] - A.Suárez, E.Ngoya, P.Savary, M.Camiade, J.C.Sarkissian, R.Quéré, "Broadband design and simulation of frequency dividers in the millimetric band", EMC-Madrid September 1993

[2] - C.Rauscher, "Regenerative frequency division with GaAs FET", IEEE MTT Vol-32 N. 11. November 1984

[3] - A.Suárez, R.Quéré, M.Camiade, E.Ngoya, "Large signal design of broadband monolithic frequency dividers", IEEE MTT Symposium Albuquerque 1992

[4] - V.Rizzoli, A.Neri, "State of the art and present trends in non-linear microwave CAD techniques", IEEE MTT Vol-36, no.2. February 1988 pp.343-365

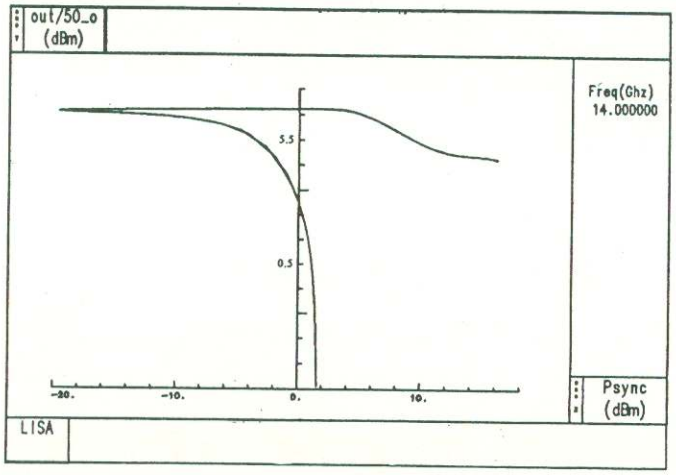

Fig.3 Output power at the divided frequency versus input power for F_{in}=28GHz

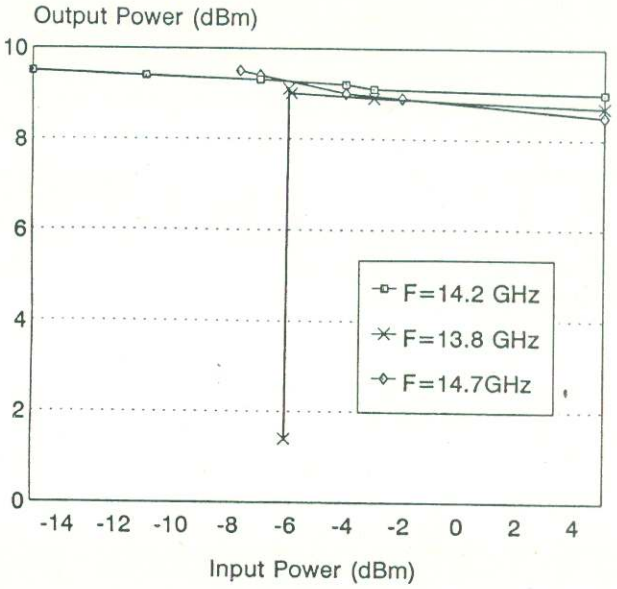

Fig.4 Measurements of power transfer characteristics

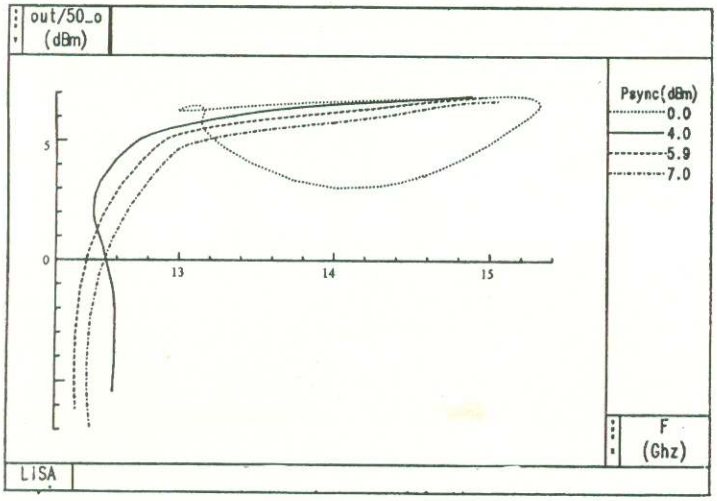

Fig.5 Simulation of synchronization bands

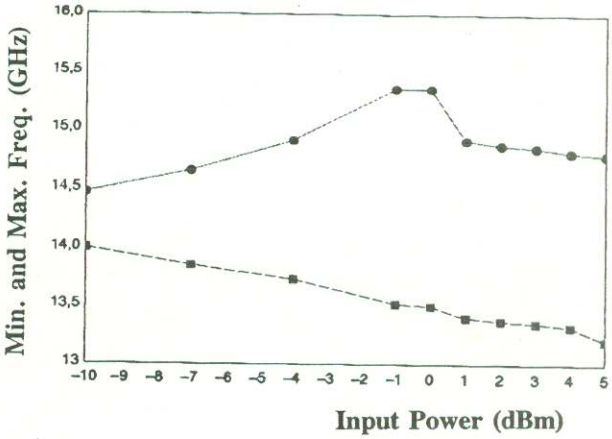

Fig.6 Experimental synchronization bands

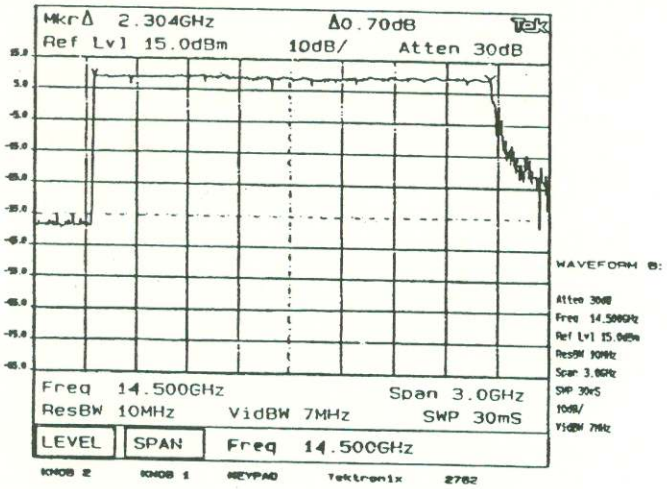

Fig.7 Output power measurement for P_{in}=0dBm