A Novel Voltage Controlled Directional Coupler Using A Wide FET Structure

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Abstract

A wide FET is considered as a voltage controlled directional coupler. A model for the device has been developed taking into account the distributed nature of the device. The six port measured and modelled S-parameters are shown to 20GHz. The results show large variation in coupling between source and drain.

Introduction

As MMIC technology has matured there has been much interest in non-standard FET structures, where the flexibility of the MMIC design process has been used to design novel devices. Wide FET's have been used as travelling wave FETs, where a growing wave propagates along the FET [1] and a Schottky contact coplanar line has been used as a voltage controlled attenuator [2]. In this work a wide FET has been configured as a four port directional coupler, where the source, gate and drain lines can be considered as coupled microstrip transmission lines and the gate bias controls the amount of coupling between source and drain. A test structure has been fabricated with a coupled length of 1.5mm and it has been shown [3] that the coupling between the source and drain can be controlled over a large frequency range. A typical wide FET structure is shown in figure 1, this chip measures 1.0mm x 3.0mm. A theoretical model of the wide FET has been developed taking into account the distributed nature of the device and the parasitics associated with mounting the device have also been included. The modelled results are compared with measured results from the test structure and good agreement has been obtained. The model has been used to investigate the effects of different gate terminations, improved performance was predicted, and has been obtained, with 50Ω loads.

Modelling

In order to understand the device operation and achieve improved performance, a model for the device has been constructed. The coupled mode method, [1], [4] is used to calculate the propagation characteristics of the device and from these the six-port Scattering parameters (S-parameters) can be derived. Firstly the static capacitances of the three electrodes are calculated. These have been evaluated using the resistive network analogue technique [5]. This technique solves the Laplacian finite difference problem by introducing resistors between the nodes of the finite difference mesh. If conducting strips are introduced into the resistive mesh, it can be shown [5] that the sum of the currents flowing into the nodes occurring on the strips is proportional to the charge density at that point. The sum of all strip node currents gives the total charge on the strip and hence the capacitance can be found. Under the Quasi-TEM approximation, the self and mutual inductances of the structure can be calculated from the static capacitances. The model is then extended by adding the intrinsic FET parameters, C_{dep}, R_{dep} and R_{ds} as distributed elements (@ I_{ds}=0). A diagram of the FET model is shown in fig. 2. The distributed immittance parameters are derived for the device and the propagation characteristics can be calculated using the coupled mode method. This analysis shows that such a three-line structure supports three possible modes, each having its own complex propagation constant. A mode impedance for each of the modes, on each of the lines is then calculated. These propagation characteristics are then used in a modal analysis which yields the scattering parameters for the six port FET structure.

Measured and Modelled Results

The FET chip measures 2.0mm x 1.0mm x 0.2mm and is mounted on a brass pedestal with tape bonds connecting the terminals to incoming microstrip lines. Initially dc was applied to the gate line via a bias resistor mounted in a high impedance line. These results are shown in fig. 3, it can be seen that at zero bias, when the channel resistance is low, the power incident on the source line splits equally between the output of the source line , S_{61} and the forward coupled port of the drain line, S_{41}, with slightly higher coupling to the backward coupled port of drain line, S_{31}. At pinch off the device acts as a set of coupled lines on a low loss substrate, with the output of the source as the through line and the drain line exhibiting backward coupling and forward isolation. The modelled results were found to agree very well with the measured results up to 20GHz. The model was then

used to find the gate terminations that resulted in the largest variation in forward coupling to the drain, these were found to be 50Ω loads. External 50Ω loads were then connected to the gate line via microstrip transmission lines and the results are shown in fig. 4. The forward transmission to the drain line , S_{41} is seen to be reduced by approximately 5dB at $V_g = -1.5V$ from 4 to 6GHz. S_{31} is slightly reduced, but still remains relatively constant. Thus an improvement in the isolation of the source and drain lines has been obtained with the addition of 50Ω loads. The transmission lines attached to the gate line have allowed the gate associated S-parameters to be measured. These are shown in fig. 5, directional coupling is again observed and they show good agreement between measured and modelled results. Thus the model shows good agreement for all eight S-parameters required to fully describe a symmetrical six port.

Conclusion

A wide FET has been shown in a new type of configuration, as a six port where the source, gate and drain are considered as three coupled lines. The coupling between source and drain can be controlled by the d.c. bias applied to the central gate line. This novel device could have many applications including distributed switching, variable power dividing or combining, variable coupling and variable phase shifters. Variable coupling has been presented, and a model of the wide FET has been developed taking into account the distributed nature of the device. Results from the model compare well with measured data. The model has been used to obtain improved performance for such devices, in terms of isolation and variation in coupling.

References

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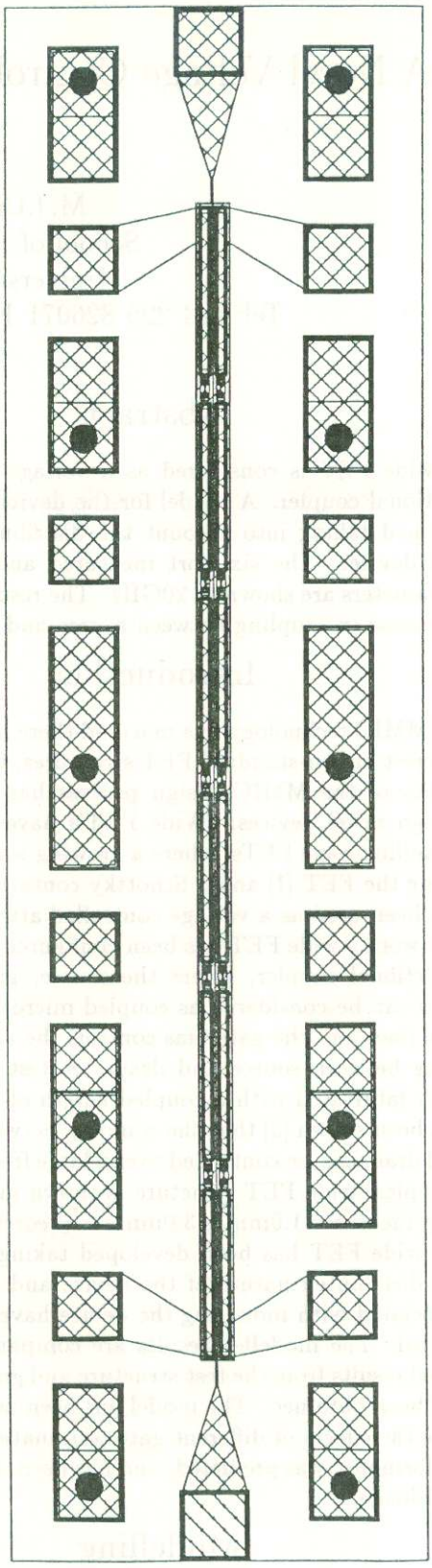

Fig 1. A wide FET structure

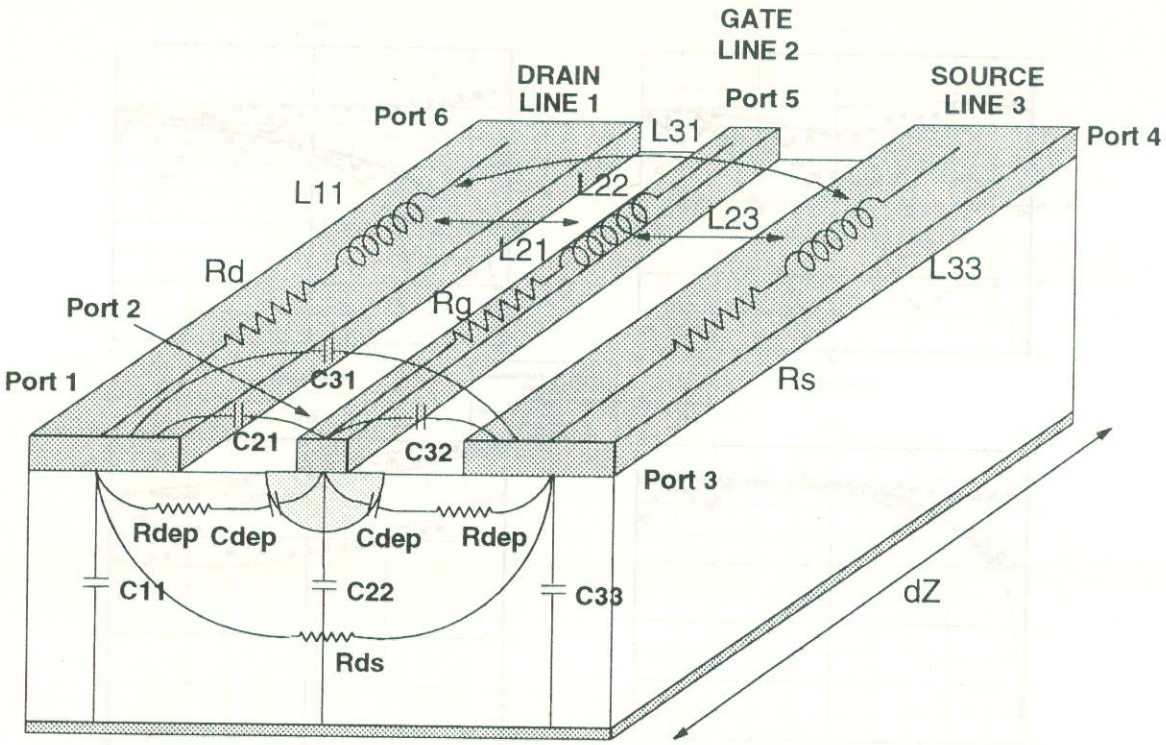

Fig 2. Unit cell for the distributed model of a wide FET structure

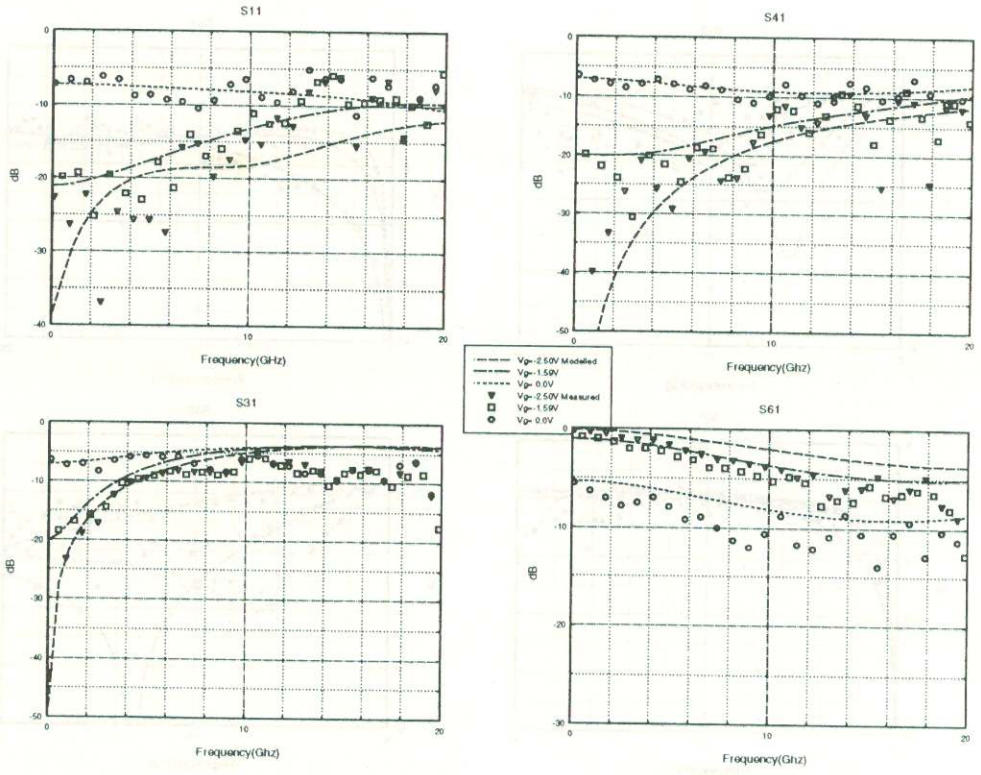

Fig 3. Measured and modelled source-drain associated S-parameters for a wide FET with an open circuited gate line.

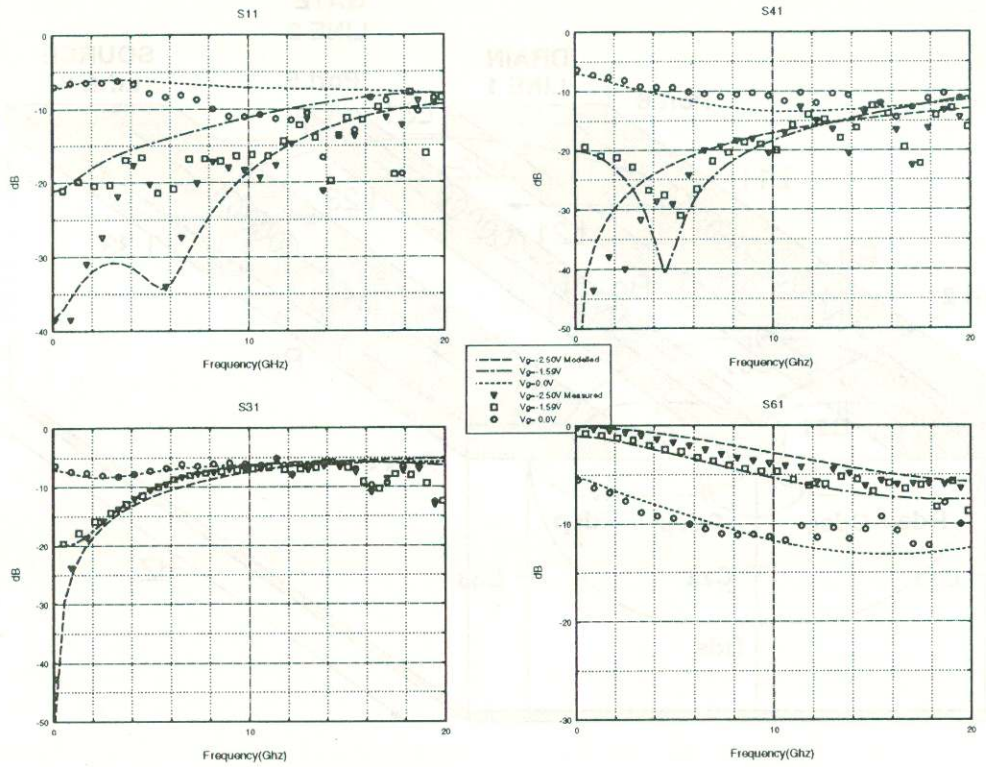

Fig 4. Measured and modelled source-drain associated S-parameters for a wide FET with 50Ω terminated gate line.

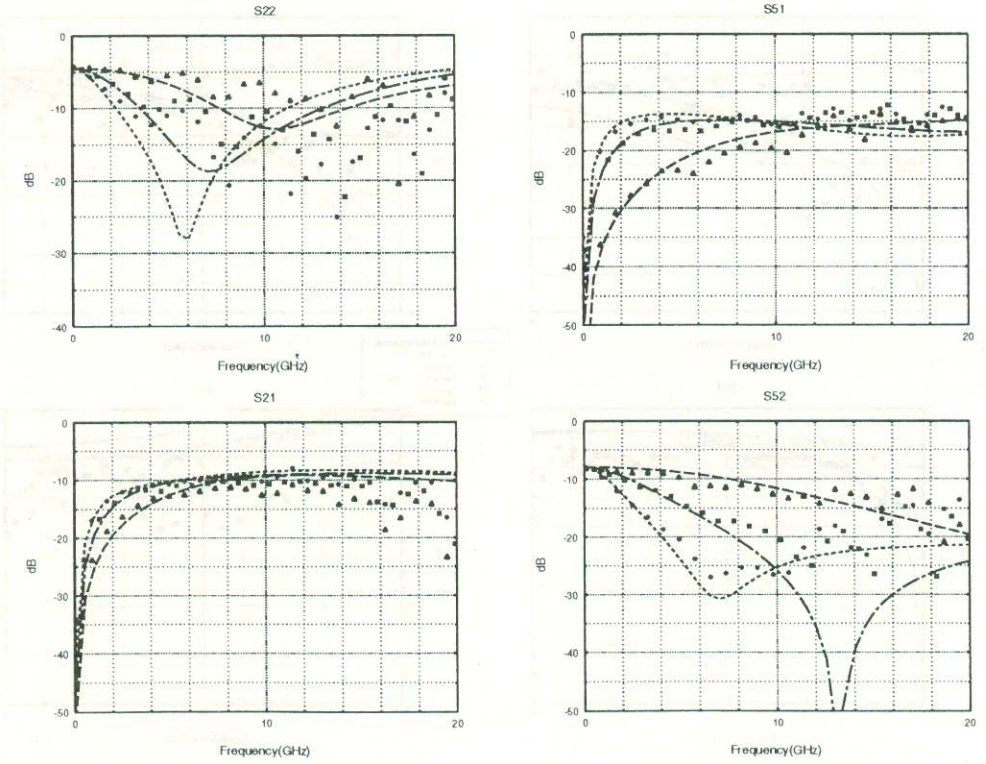

Fig 5. Measured and modelled gate associated S-parameters for a wide FET with 50Ω terminated gate line.