Modelling & Characterisation of a Ka-band Monolithic PHEMT Low-Noise Feedback Amplifier

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Abstract

The modelling and test of a single stage and a two-stage monolithic millimetre-wave (Ka-Band) pseudomorphic HEMT feedback amplifier is reported. The amplifiers used 0.25μm x 120μm devices and were processed on 200μm thick GaAs wafers. The PHEMT s-parameters were measured on-wafer to 40GHz in conjunction with on-wafer Line-Reflect-Line (LRL) calibration standards, which are described. The amplifier modelling approach combined a device equivalent circuit model with a fullwave analysis of the microstrip features and selected measurement-based foundry models. Measured and fitted data are compared for the PHEMT device and for the amplifiers. A single stage feedback amplifier gain of 7.8dB was measured at 33.8GHz and a two-stage feedback amplifier gain of 13.2dB $\pm$ 0.4dB from 28.6GHz to 37.9GHz. Both measurements were in good agreement with simulations. The on-wafer measured noise figure of the two stage amplifier was 3.4dB at 35GHz.

Introduction

The emergence in recent years of the GaAs/AlGaAs high-electron-mobility transistor (HEMT) and the InGaAs/AlGaAs pseudomorphic HEMT, with gate lengths as small as 0.1μm, has opened up monolithic technology to a wide range of mm-wave system applications. For the mm-wave system designer, however, the luxury of selecting a commercially available chip to fully meet his/her requirements is not yet a reality. More often than not, an expensive custom design must be pursued so making "first-pass success" an important criterion. However, the available data base for circuit simulation is often limited and simulation tools in some cases are not fully proven. Success depends very much on the accuracy of the models that are employed in the design process and on the closeness of the agreement between measurements and simulations.

The work reported here covers the characterisation and modelling of a 0.25μm x 120μm pseudomorphic HEMT and the modelling and test of Ka-band monolithic amplifiers on 200μm thick GaAs substrates. The processing was performed by GEC Marconi Materials Technology. In developing good mm-wave device models, accurate on-wafer s-parameter measurements are of paramount importance. For the work herein described a 40GHz wafer prober was employed which, in conjunction with custom designed on-wafer microstrip calibration standards, provided excellent data for the development of linear circuit simulation models to 40GHz.

Device Characterisation & Modelling

The development of good a.c. equivalent circuit models relies on the availability of two-port scattering parameters which accurately describe the device performance. Such data can be obtained either analytically from a physics based model, if available, or can now be measured on-wafer to circa 100GHz using coplanar wafer probes. The latter approach was adopted for this work and its success relied on accurate on-wafer s-parameter measurements being made on microstrip-fed devices to 40GHz. On-wafer microstrip calibration standards were developed and used in conjunction with a Hewlett Packard 45MHz to 40GHz Network analyser and a Cascade Model 44 wafer prober to make error corrected s-parameter measurements. Ground-Signal-Ground (GSG) probes were used with 200μm pitch.

Coplanar waveguide (CPW) calibration standards for wafer probing are well established in a variety of calibration schemes to around 100GHz and Schlechtweg *et al* [1,2] have demonstrated good agreement between measured and modelled devices & circuits in coplanar waveguide (CPW) to 75GHz. However, accurate s-parameter measurements of microstrip-fed devices on-wafer are not yet routine at millimetre wave frequencies, although the measurement equipment is well established. Microstrip-fed device models are often generated from measurements on CPW fed devices. These data can lead to a useful microstrip based model but the CPW configuration has different embedding parasitics, lower source inductance, and a differing surrounding electric field. These differences can lead to a microstrip-based model which may fit the data but which may not accurately differentiate between the embedding parasitics and the intrinsic device parameters. Such a model cannot always be confidently scaled. To define the intrinsic s-parameters of a microstrip fed device it is usually necessary to de-embed the effect of a coplanar-waveguide-to-microstrip transition, necessitated by the use of CPW wafer probes in conjunction with an off-wafer CPW calibration. To avoid transition de-embedding and its associated uncertainties, our approach was to measure the device in a configuration that would subsequently be employed within the specified amplifier (sources via-grounded). Microstrip on-wafer line-reflect-line (LRL) calibration standards were developed [3,4] which included the transition in the calibration and removed the need to de-embed its effect. Measurement reference planes were shifted to the device terminals using the intrinsic analyser software.

Figure 1 shows the microstrip LRL calibration standards, located in five process control monitor (PCM) sites across each processed wafer. A pair of via-grounded pads either side of the input/output microstrip feeds interfaced with the applied GSG wafer probes. This transition was designed not only to be compatible with the measurement and calibration scheme, but also with the proposed packaging concept - namely, that the transition should have minimal effect on the line impedance when used in isolation on a diced chip. A 3D analysis of the proximity effect of the grounded pad indicated that the impedance was locally reduced by approximately 15% for closely spaced vias compatible with 200μm pitch probes. The transition linewidth was reduced to compensate for this effect. The quality of the on-wafer calibration was validated by measurements on a long open-circuited microstrip line, although no verification standards are available to fully endorse them. Prototype standards initially demonstrated a resonance at circa 27GHz but this was removed on subsequent designs by providing a greater spacing between standards. It is believed that the resonance was due to coupling from the underside of the CPW probes to nearby substrate metallisation.

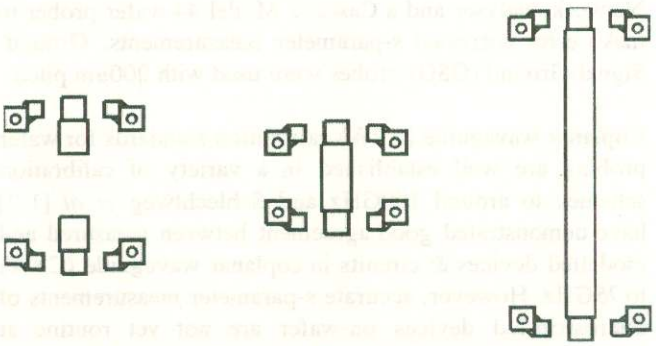


Figure 1: Microstrip LRL Calibration Standards

Several batches of prototype device wafers were characterised to 40GHz and the proprietary fitting software FETlink was used to fit batch equivalent circuit models to the measured PHEMT data. A conventional FET equivalent circuit model was used. A 3D electromagnetic simulator was employed to analyse the embedding feeds and a simple LC model fitted to the data to represent the input/output feeds. This analysis was backed up with measurements on a "cold" device. The via-hole source inductance was measured on wafer and shown to be 48pH.

In order to realise a batch model that had minimal spread on its parameters, and one which accurately represented the typical device, fitting was initially restricted to devices that fell within a $\pm 5\%$ window of the average I_{dss} across the wafer. Figure 2 compares typical PHEMT measured data for the PHEMT with the FETlink model. Subsequent analysis showed that the model also provided a reasonable fit to devices with $\pm 10\%$ variations in I_{dss}. Good scaling properties were observed for the intrinsic model when comparisons were made with devices of differing gate widths.

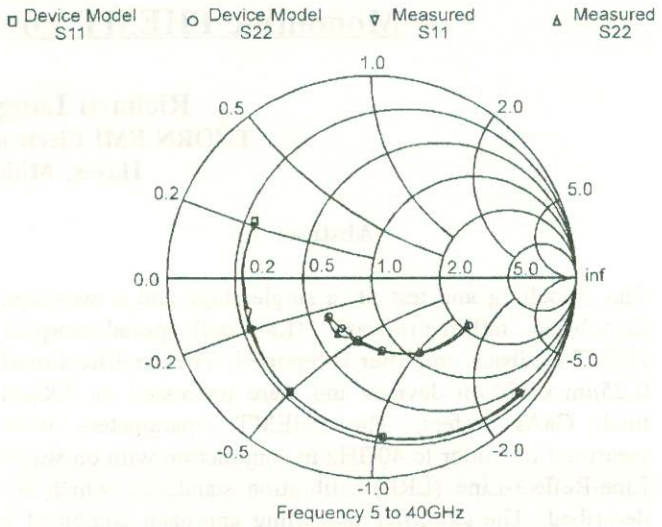
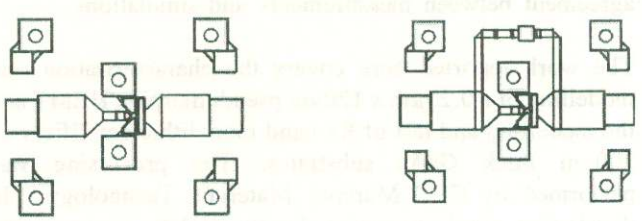


Figure 2: Measured and Modelled PHEMT S11 & S22

Circuit Design and Modelling

A feedback configuration was used to reduce the amplifier sensitivity to variations in device parameters from batch to batch. The design approach was to use equivalent circuit models for the PHEMT devices, foundry data for the transmission lines (based on resonator measurements to 40GHz), and to employ fullwave analysis for the microstrip components and discontinuities wherever possible. A linear circuit simulator was used to simulate and optimise the amplifier using these externally developed models. The analysis was segmented and the layout was constrained to avoid coupling between circuit elements - this removed the need for full 3D modelling of portions of the circuit. However, the feedback loop around the device was only 0.5h from the device and coupling effects were expected to modify the device & feedback characteristics. To study this effect, a "feedback cell" was processed on the same wafer as the amplifier as a building block for post-fabrication diagnostics. The layout of the basic PHEMT device and the feedback cell are shown in figure 3.



a) Standard Device b) Feedback Cell

Figure 3:Layout of PHEMT Devices

Figure 4 shows the layout of the single stage feedback amplifier. This amplifier was designed primarily as a vehicle for proving the modelling approach but was also the basic building block of the two-stage amplifier. Its dimensions are 2.5mm x 2.4mm. Figure 5 shows the layout of the two-stage amplifier. This chip measures 4.6mm x 2.4mm.

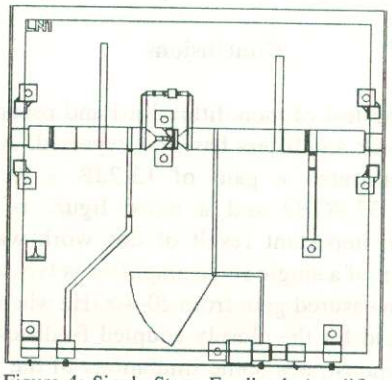


Figure 4: Single Stage Feedback Amplifier

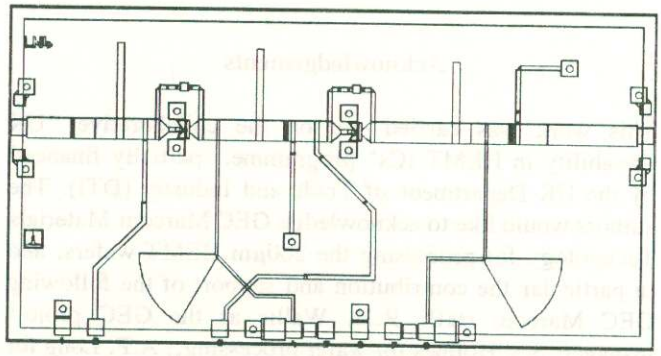


Figure 5: Two stage PHEMT Feedback Amplifier

Amplifier Measurements

Figure 6 is a comparison between measured (on-wafer) and modelled gain for the single stage feedback amplifier. The measured gain is 7.8dB at 33.8GHz. MODEL1 is the initial simulation which uses a segmented feedback loop around the device model. MODEL2 is a post-fabrication simulation which uses the measured data for the "feedback cell". The MODEL1 simulation deviates as much as 1dB from the measured data. However, the MODEL2 simulation is typically within 0.3dB of the measured data from 20-40GHz. Figure 7 and Figure 8 show the measured and modelled S11 and S22. Both models gave reasonable agreement with measured mag[S11] and the modelled mag[S22] minima was within 2.6% of the measured performance. The comparison shows that in this example of a feedback amplifier, the segmented analysis of a close proximity feedback loop can provide a moderate fit to measured performance but if better accuracy is required, then either measured "building block" data or a 3D analysis of the device embedding networks should be employed.

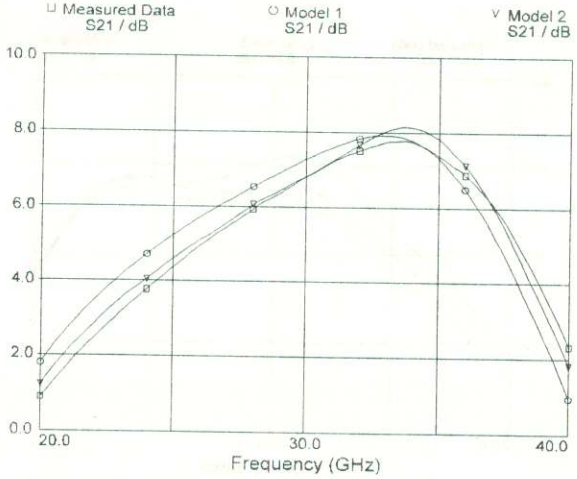


Figure 6: Measured & modelled S21 of a single stage amplifier

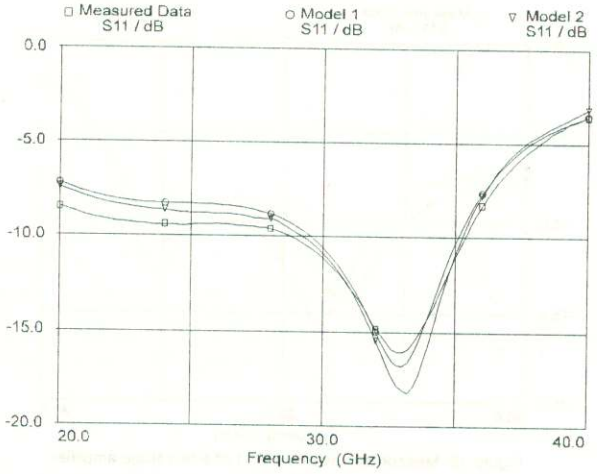


Figure 7: Measured & modelled S11 of a single stage amplifier

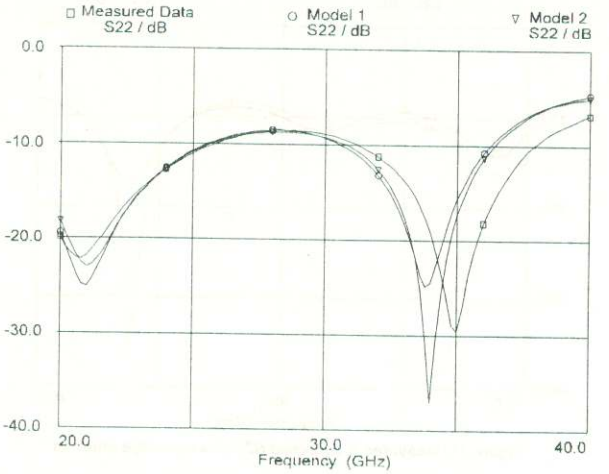


Figure 8: Measured & modelled S22 of a single stage amplifier

Figure 9 compares modelled and measured S21 of a two-stage amplifier. MODEL3 is the segmented simulation, as previously described for the single stage amplifier. MODEL4 uses the measured feedback cell data.

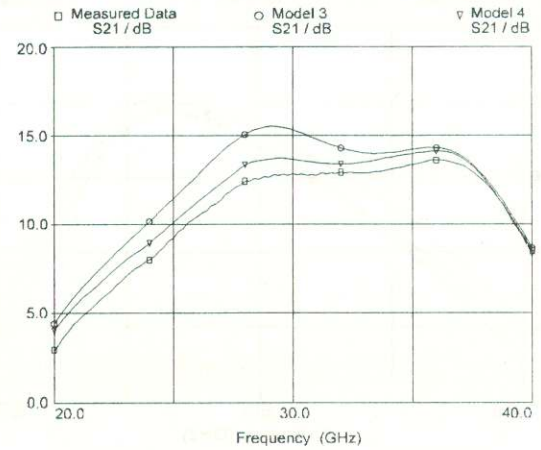


Figure 9: Measured & modelled gain of a two stage amplifier

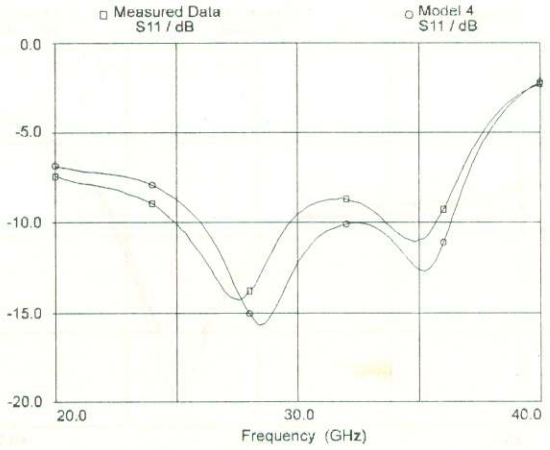


Figure 10: Measured & modelled S11 of a two stage amplifier

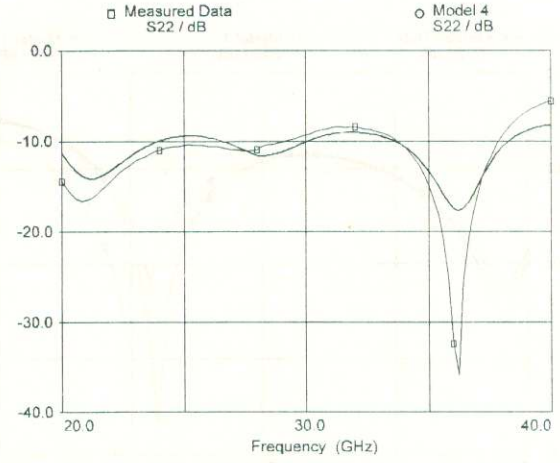


Figure 11: Measured & modelled S22 of a two stage amplifier

Figures 10 & 11 show measured and simulated S11 & S22, with the poorer MODEL3 omitted for clarity. Overall, the MODEL4 simulation shows close agreement with the measured data, demonstrating a gain of 13.2dB $\pm$ 0.4dB from 28.6GHz to 37.9GHz. The segmented simulation gives a 2.7dB higher gain prediction. The two-stage amplifier noise figure was also measured on-wafer and a swept measurement indicated a noise figure of 3.4dB at 35GHz.

Conclusions

The design and test of monolithic Ka-Band pseudomorphic HEMT feedback amplifiers has been reported. A two-stage design demonstrated a gain of 13.2dB $\pm$ 0.4dB from 28.6GHz to 37.9GHz and a noise figure of 3.4dB at 35GHz. The important result of this work was that the simulated gain of a single stage amplifier is typically within 0.3dB of the measured gain from 20-40GHz when measured data is included for the closely coupled feedback network. The work demonstrates some limitations of the segmented type simulation when applied to closely coupled millimetre-wave circuit structures and further confirms the need to consider using 3D electromagnetic analysis in such circuits.

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