Systematic Design of MMIC Broad Band 90° Phase Shifters

M. Mahfoudi and José I. Alonso.

Dpto. de Señales, Sistemas y Radiocomunicaciones.
E.T.S.I. de Telecomunicación. U.P.M. 28040 MADRID

Abstract

This paper describes a systematic method to design wideband 90° phase shifter circuits to be implemented using MMIC technology. The circuit structuresare based on the combination of two RC-all pass filters, and the proposed method allows the computation of circuit elements in a simple manner for minimum phase shift and amplitud errors over any frequency range. One of the RC-all pass filter structure is an active structure which has no losses. A 90° phase shifter circuit has been designed using this method, the phase shift errror and amplitud error are 2° and 1 dB over more than two octave bandwidth, (0.8 - 4.8 Ghz).

I. Introduction

Because of the great interest in monolithic 90° phase shifter IC's at microwave frequency range [1], many novel circuit techniques has been proposed for its implementation using the advantages of GaAs MMIC technology [2], [3], [4]. The RC all-pass filters option reveals yielding wider shift band and most suitable for monolithic implementation.
The basic configuration consists of two all-pass filters driven in parallel. Although the design principles are well known [5], [6], the application of these principles was cumbersome and ambiguous with regard to the match of the two circuit components to give 90° phase difference within some prescribed error while the amplitudes must remain equal. Hence from a practical point of view, is necessery a simple method of designing 90° phase shifters for any specifications. This paper gives a systematic design of phase shifters based on two configurations of RC all-pass filters [7].

II. RC All-Pass Filter structures

A. Passive RC All-Pass Filter

The structure is given in fig. 1. Since it is a balanced structure, it requires an additional stage in order to achieve a common output ground. However, for many applications a balanced structure would be desirable to permit integration with other blocks [8]. Furthermore, this configuration use only few resistors and capacitors, so it is more suitable for high frequency range applications requiring small size and low power. The structure drawback is the voltage transmission loss.

B. Active RC All-pass Filter

The structure is given in fig. 2. This configuration avoids the transmission loss problem without requiring baluns or transformers and it offers the possibility of tuning the response.

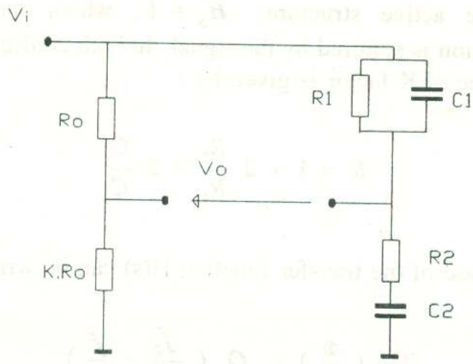

Fig. 1. Passive RC All-Pass filter

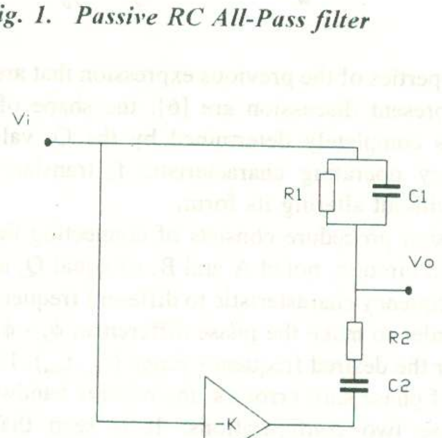

Fig. 2. Active RC All-Pass filter

III. Design Principles

The voltage transfer function for the two configurations can be expressed as follows:

$$H(s) = H_o \cdot \frac{\left(\frac{s}{w_o}\right)^2 - \frac{1}{Q_o} \cdot \frac{s}{w_o} + 1}{\left(\frac{s}{w_o}\right)^2 + \frac{1}{Q_o} \cdot \frac{s}{w_o} + 1} \qquad (1)$$

where:

$$s = j \cdot w \qquad w_o^2 = \frac{1}{R_1\, C_1\, R_2\, C_2} \qquad Q_o = \frac{\sqrt{\frac{R_2}{R_1} \cdot \frac{C_1}{C_2}}}{1 + \frac{R_2}{R_1} + \frac{C_1}{C_2}}$$

The constant H_o is different for each configuration, In the passive structure, its value are given by :

$$H_o = \frac{1}{2 + 2\,\frac{R_2}{R_1} + 2\,\frac{C_1}{C_2}} \qquad (2)$$

For the active structure, $H_o = 1$, which means no attenuation is suffered by the signal. In both configurations the value of K factor is given by :

$$K = 1 + 2\,\frac{R_2}{R_1} + 2\,\frac{C_1}{C_2} \qquad (3)$$

The phase of the transfer function H(s) can be written as :

$$\tan\left(\frac{\phi}{2}\right) = Q_o \left(\frac{f_o}{f} - \frac{f}{f_o}\right) \qquad (4)$$

The properties of the previous expression that are important to the present discussion are [6]: the shape of the phase curve is completely determined by the Q_o value and the frequency operating characteristic f_o translate the phase curve without altering its form.

The design procedure consists of connecting the inputs of two such circuits, noted A and B, of equal Q_o and to tune their frequency charasteristic to different frequencies, f_A and f_B, in order to make the phase difference, $\phi_A - \phi_B$, closed to 90° over the desired frequency range (f_{min},f_{max}). Fig. 3 shows a plot of phase shift error vs. the relative bandwidth f_{max}/f_{min} for these two configurations. It is seen that even for adecade bandwidth the theoretic phase shift error is 1°.

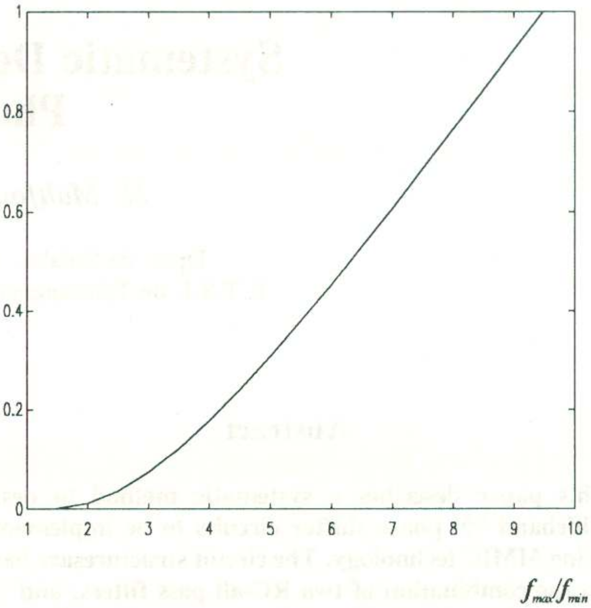

Fig. 3. Phase shift error vs. relative bandwidth

IV. Systematic Design

The developed design method only requires the frequency limits, f_{min} and f_{max}, of the work band. Two parameters, p and r, are directly found from the plot of fig. 4. The p parameter is given by:

$$p = \frac{R_2}{R_1} = \frac{C_1}{C_2} \qquad (5)$$

and r is a factor which assure that the phase deviations with respect to 90° are always equals and minima. Given these parameters, the optimum component values are calculated as follows :

$$R_{1A} = \frac{R_{2A}}{p} \qquad C_{1A} = \frac{r \cdot p}{2\,\pi\,\sqrt{f_{max} \cdot f_{min}}\; R_{2A}} \qquad C_{2A} = \frac{r}{2\,\pi\,\sqrt{f_{max} \cdot f_{min}}\; R_{2A}} \qquad (6)$$

$$R_{1B} = \frac{R_{2B}}{p} \qquad C_{1B} = \frac{p}{2\,\pi\,r\,\sqrt{f_{max} \cdot f_{min}}\; R_{2B}} \qquad C_{2B} = \frac{1}{2\,\pi\,r\,\sqrt{f_{max} \cdot f_{min}}\; R_{2B}}$$

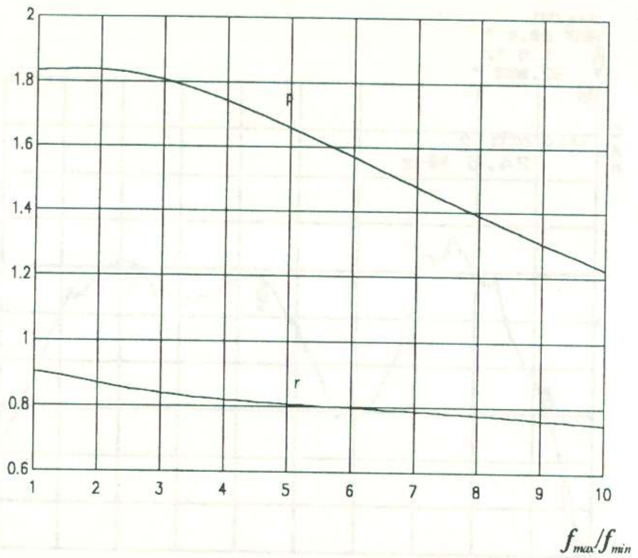

Fig.4. Design parameters vs. relative bandwidth

The choice of R_{2A} and R_{2B} values is based on technology restrictions.

V. Circuit Implementation

To check the validity of the proposed design approach a phase shifter circuit corresponding to the active structure has been designed and measured to operate over the frequency range 0.8 - 4.5 Ghz.
Since f_{min} = 0.8 Ghz and f_{max} = 4.5 Ghz, from fig. 3 the theoretic phase error is 0.5° and from fig. 4, r = 0.6 and p = 1.6. The calculated component values are :

$$\begin{array}{llll} R_{2A} = 295.5\ \Omega & & R_{2B} = 397.7\ \Omega & \\ R_{1A} = 159.7\ \Omega & & R_{1B} = 215.8\ \Omega & \\ C_{1A} = 0.82\ pF & & C_{1B} = 0.19\ pF & \\ C_{2A} = 1.82\ pF & & C_{2B} = 0.42\ pF & \end{array} \tag{7}$$

The gain of the active stage gain is K = 4. The practical circuit is implemented as a common source 0.5 μm-gate-length MESFET's amplifier. Two input/output matching stages were added in order to measure the circuit. The schematic of the circuit is shown in fig. 5. A resistor in each one of the two all-pass circuit, have been replaced by voltage-controlled variable resistors, allowing to introduce a phase correction, to compensate possible errors. These variable resistors are made using a "cold" FET (FET without drain bias, that works in the ohmic region). The variable resistors are implemented instead of the resistors R_{1A} and R_{1B}. The resistors R_{2A} and R_{2B} are simulated as the active stage output resistances. The circuit layout is shown in fig. 6. Fig. 7 and 8 show the simulated performance, using the program LIBRA of EEsof Inc. All the parasitics, including transmission lines and equivalent circuit for passive elements, were introduced in the simulation.

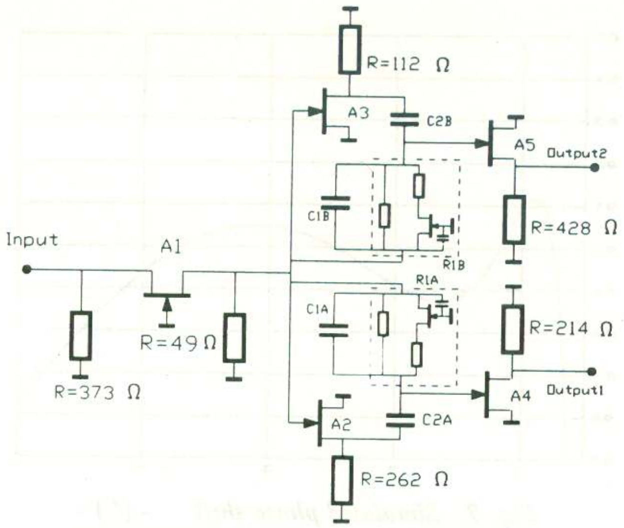

Fig.5. Circuit schematic

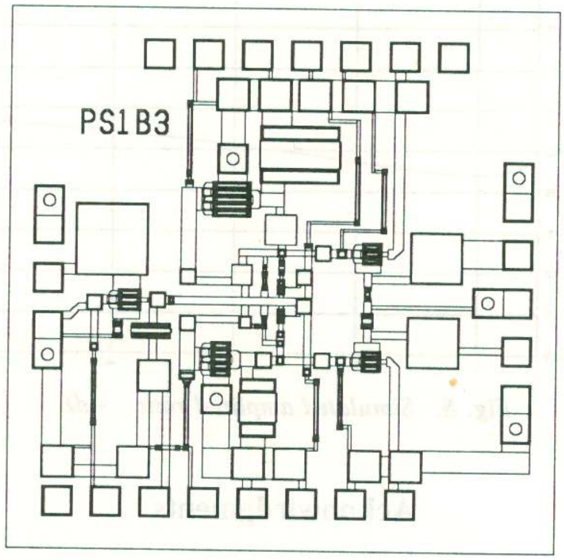

Fig. 6. Circuit layout

Figures 9 and 10 show the measured performance resulting in 2° maximum phase shift error and 1 dB maximum amplitude ratio error over a wide frequency range 0.8 - 4.8 Ghz. The DC bias provides a precise tuning of the phase shift and amplitude ratio errors to 0.5° and 0.1 dB for 200 Mhz bands within the range 0.8 - 4.8 Ghz.

V. Conclusion

An accurate method for 90° phase shifters design has been presented. It's intented to simplify the use of RC all-pass techniques at higher frequencies on GaAs technology. The results shown that wideband phase shifter circuits with satisfactory performances can be designed.

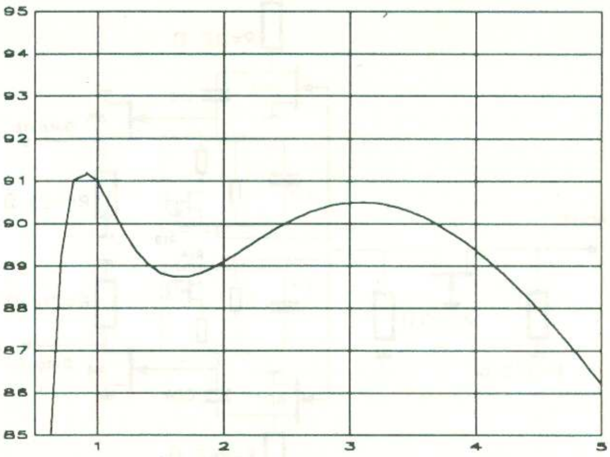

Fig. 7. Simulated phase shift - (°) -

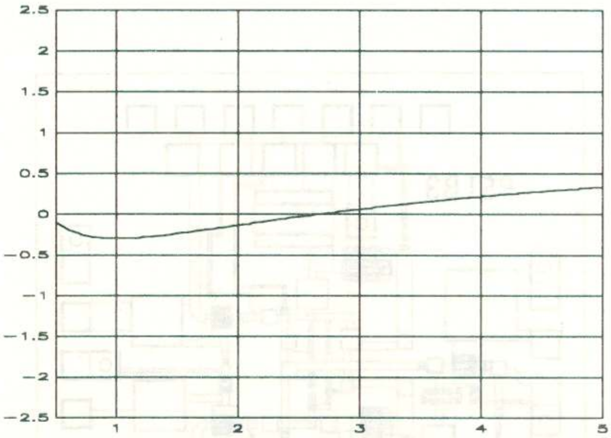

Fig. 8. Simulated amplitud ratio - dB -

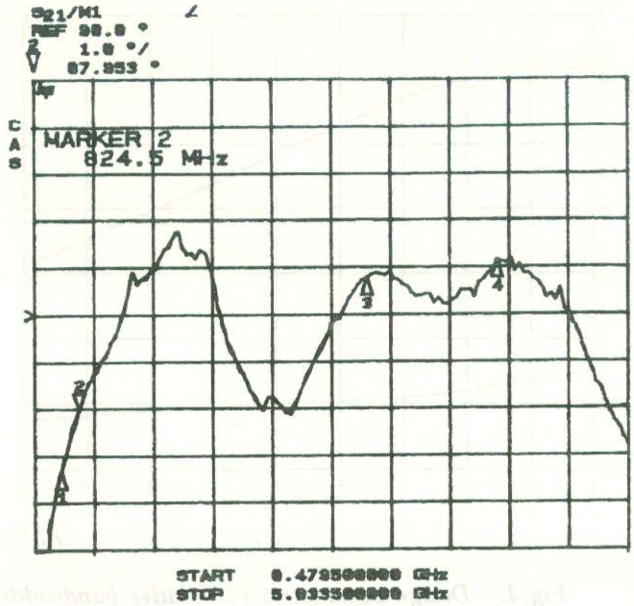

Fig. 9. Measured phase shift - (°) -

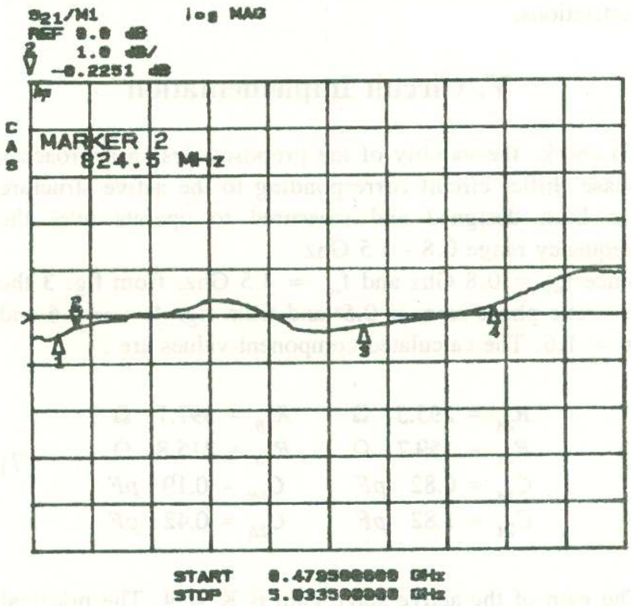

Fig. 10. Measured amplitud ratio - dB -

Acknowledgments

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