Harmonic Manipulation Cure for High-Efficiency Power Amplifiers

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Abstract

A straightforward synthesis method for the optimisation of harmonic loading of high-efficiency class-AB microwave power amplifiers is presented. Amplitudes of harmonics are determined that optimise the output voltage and current waveforms in a realistic case; simple formulae are given for the synthesis of the loads. Results and comparisons with a standard design are presented that show the improvement in output power and efficiency.

Introduction

It is well known that harmonic control techniques can improve the performance of a power amplifier [1]; a theoretical analysis shows that the optimum output voltage waveform for a high-efficiency class-B amplifier is a square wave. If perfect short- and open-circuit terminations at even and odd harmonics respectively are assumed, the voltage waveform is constrained to be approximately squared for a high drive level by the non-linearities of the active device, *i.e.* breakdown, pinch-off, forward gate conduction, etc. that thereby determine its harmonic content.

In a practical case ideal open circuits cannot be obtained because of the presence of the (nonzero) output conductance of the device; since the harmonics of the current are generated by the non-sinusoidal current already at moderate drive levels for class-AB amplifiers, harmonics of the voltage are present before the limiting physical phenomena take place. If the device is suitably loaded at harmonic frequencies, the output voltage can be shaped to an approximately square wave; provision must however be done for the fact that it is difficult to control harmonics higher than the third. A straightforward synthesis method for harmonic loading is hereafter presented, that yields an improvement of output power and efficiency of the power stage over a standard design.

The synthesis method

A first requirement is that the output be tuned at all frequencies, *i.e.* that all harmonic loads be purely resistive (short circuit included) [1][2], so that the (truncated sinusoidal) current and the (approximately square) voltage waveforms be in phase opposition at the drain of the transistor. Output characteristics as in Fig. 1 are assumed for the analysis.

The main problem is the approximation of the ideal drain voltage square waveform with only fundamental and third order components:

$$V_{DD} + V_{MAX}\frac{4}{\pi}\sum_{n=0}^{\infty}(-1)^n\frac{\cos[(2n+1)\omega t]}{2n+1} \approx$$

$$\approx V_{DD} + V_{ds,1}\cos(\omega t) - \varepsilon V_{ds,1}\cos(3\omega t)$$

where

$$\varepsilon \equiv -\frac{V_{ds,1}}{V_{ds,3}} = -\frac{R_1}{R_3}\frac{I_{ds,1}}{I_{ds,3}}$$

and R_1, $I_{ds,1}$, $V_{ds,1}$, R_3, $I_{ds,3}$, $V_{ds,3}$ are the load, the drain current and drain voltage components at the fundamental and third harmonic, respectively. It is possible to show that for a given V_{max} (i.e. the maximum excursion of the drain voltage, normally bounded by the hard limits of the transistor operation, breakdown and/or ohmic behaviour), the drain voltage normalised fundamental component can be adequately described via the relation:

$$\frac{V_{ds,1}}{V_{MAX}} = \frac{1}{cos[\vartheta(\varepsilon)] - \frac{cos[3\vartheta(\varepsilon)]}{\varepsilon}} = \gamma(\varepsilon)$$

where

$$\vartheta(\varepsilon) = asin(\sqrt{\frac{9-\varepsilon}{12}})$$

shown in Fig. 2, clearly indicating the allowable values for ε and its optimum values ranging from 5 to 7.

The value of third harmonic load conductance which realizes the desired value for ε, normalized to the load at the fundamental, can be found from a current waveform analysis to be:

$$\frac{G_3}{G_1}(\vartheta_x, \varepsilon) = -\frac{sin(\vartheta_x)[1 - cos(\vartheta_x)]}{3[\vartheta_x - sin(\vartheta_x)]}\varepsilon \qquad (1)$$

where ϑ_X is the conduction angle, defined as

$$\vartheta_x = 2acos(\frac{I_{bias}}{I_{MAX} - I_{bias}})$$

Indicating with $\mathbf{R_L}$ the optimum load for the case of all harmonics shorted [2], the load to be presented at the fundamental frequency results to be

$$R_1 = \frac{V_{1Max}}{I_{ds,1}(\vartheta_x)} = \frac{\gamma(\varepsilon)V_{MAX}}{I_{ds,1}(\vartheta_x)} = \gamma(\varepsilon)R_L$$

Hence, from (1) the load at the third harmonic is chosen. We must remember that these values for first and third harmonic resistances include the output resistance of the active device (Fig. 1); the actual external resistance must be such that its parallel with the output resistance give the desired load. If the output resistance is lower than the value to be synthesised, a non-optimum loading results.

It is possible now to evaluate output quantities (output power P^{3rd}, power gain G^{3rd}, power-added efficiency PAE^{3rd}) and estimate the obtainable improvement with respect to the case of all harmonics shorted (quantities with the superscript SH):

$$P^{3rd}_{out} = \gamma(\varepsilon)P^{SH}_{out}$$

$$G^{3rd}_{P} = \gamma(\varepsilon)G^{SH}_{P}$$

$$PAE^{3rd} = PAE^{SH} + (\gamma(\varepsilon) - 1)\eta^{SH}_{D}$$

where η_D is the drain efficiency.

Results

In order to demonstrate the effectiveness of the proposed design methodology, a previously designed power stage has been optimised. The results of this optimisation are shown in Fig. 3: the left plot shows the performances of a power stage at 10 GHz designed imposing short circuits at all harmonics and the right plot is relative to the case of harmonic manipulation. Solid lines are full nonlinear simulations (LIBRA, from EEsof) obtained after a simulated Load-Pull technique, and dots are the design points according to the proposed design procedure. The improvement is of the order of 15%, as well known from practical examples; agreement with the more elaborate non-linear simulation is very good.

Conclusions

A straightforward method for the synthesis of high-efficiency optimally-loaded microwave power amplifiers has been presented. Harmonic loading only up to the third harmonic and the effect of the output reactance have been included. Comparison with full non-linear commercial CAD package confirm the validity of the proposed approach.

References

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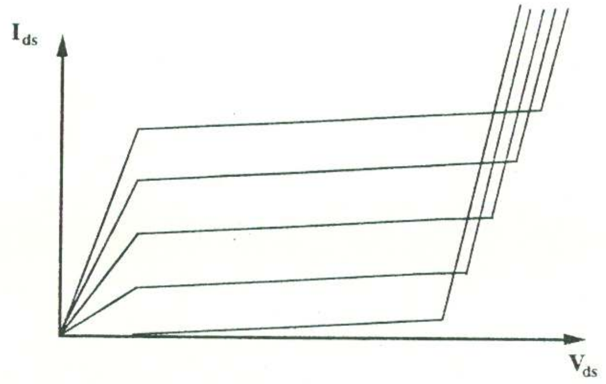

Fig. 1 - The output characteristics including the output conductance

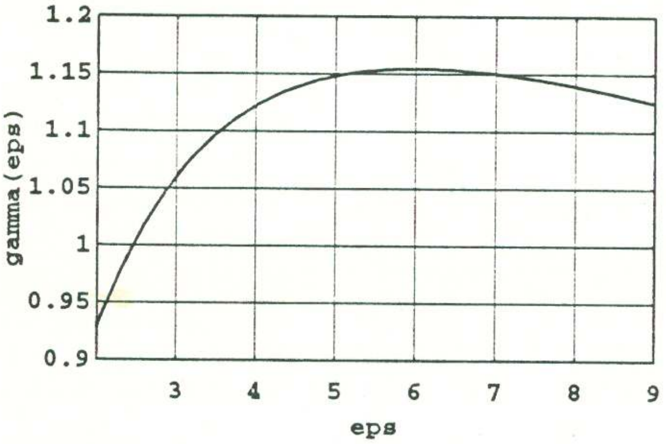

Fig. 2 - First harmonic to maximum voltage ratio as a function of first-to-third harmonic voltage ratio

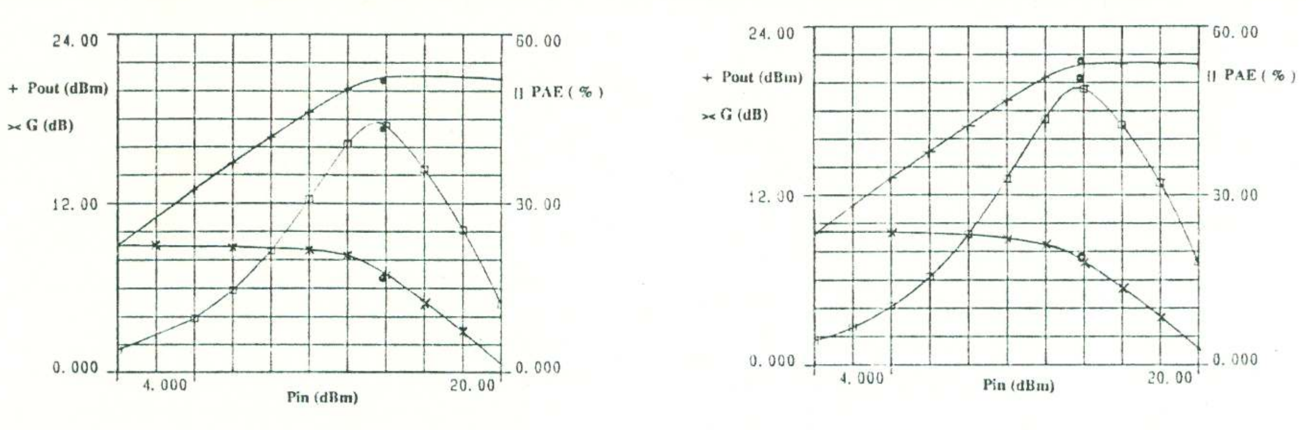

Fig. 3 - Output power, power gain and power-added efficiency for a standard (left) and improved (right) design; full non-linear analysis (solid line) and our method (dots)