A large-scale, self-consistent thermal simulator for the layout optimization of power III-V field-effect and bipolar transistors

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Abstract

The paper describes the application of a 3D large-scale thermal simulation tool to the layout analysis and optimization of power III-V devices. A short description is provided of the hybrid algorithm (Green's function and finite-element) exploited by the simulator. The model accounts for non-linear multilayered substrates, heat conduction through surface metallizations and via holes, and substrate thinnings. Case studies are discussed to demonstrate the effectiveness of the approach in investigating the thermal behaviour of different device layouts.

Introduction

The thermal optimization of compound semiconductor field-effect (FETs) and heterojunction bipolar (HBTs) power transistors has been for years a matter of concern to device designers. Although the goal of thermal design is well understood, the application of the different heat sinking procedures available requires to establish a tradeoff between the complexity and cost of technological processes (such as those related to the manufacturing of source vias, localized substrate thinnings, and thick metallizations) and the real benefit that will be finally achieved from them. Thus, the combined use of different heat sinking strategies should be carefully studied not only to appreciate their real impact on device cooling, but also to allow the designer to optimize the available heat sinking structure. A comprehensive CAD tool able to derive the detailed large-scale surface temperature distribution for a realistic device would enable the optimization of the layout and of the heat sinking prior to device manufacturing, and would also suggest possible ways to improve the thermal design.

Despite the continuous interest devoted during the last few years to the thermal simulation of compound semiconductor devices and integrated circuits, an efficient, accurate and comprehensive CAD approach to the large-scale thermal simulation is not available yet to the designer. As in other fields of physics-based modelling, very accurate models are far too computationally intensive to be exploited in the 3D analysis of large power devices, while efficient and simplified thermal analysis methods fail to provide reliable temperature estimates in realistic conditions. A reasonable compromise has to be sought for, in which all the essential features of accurate physics-based models are retained, while approximations are made to preserve computational efficiency.

To introduce the technique proposed in the paper, a short review of the available thermal analysis methods is in order. Accurate self-consistent physics-based electrothermal models have been proposed both for FET and for HBT analysis (see *e.g.* [1, 2]). Although such models allow for the microscopic interaction between thermal and electrical phenomena (such as carrier transport), the high computational intensity restricts their use to the small-scale simulation of the active region of the device. On the other hand, a number of analytical and numerical techniques (sometimes coupled to simplified electrical models to obtain a self-consistent heat distribution) are available for large-scale thermal device analysis. Thermal resistance models [3, 4, 1] provide an estimate of the average temperature of the device, but uncorrectly assume that the regions of the device wherein power is dissipated are isothermal. As well known, this approximation considerably affects the detailed temperature profile near the temperature peaks, and leads to the need for empirical adjustments (such as introducing an equivalent heat source width) to match experimental data. High-resolution surface temperature distributions can be derived from Green's function approaches at a moderately high computational cost, starting from a known dissipated power density. Often the power density is assumed to be piecewise constant [5, 6, 7], although this assumption may be questionable, above all in HBT's. Recently, T-dependent, self-consistent distributed heat sources coupled to Green's function techniques was used for HBT analysis [8, 9, 10]; the issue has been sparsely addressed also for FETs, see [11].

Many classical CAD tools based on the implementation of either finite-difference (FDIFF) or finite-element (FEM) techniques are commercially available for the thermal simulation of three-dimensional, arbitrarily shaped structures. Such tools have been widely used also for the simulation of semiconductor devices; however, despite their geometrical flexibility (which allows for the inclusion of heat conduction through metallic electrodes [12]), the computational intensity is still too large to enable the analysis of realistically complex device layouts.

Thus, it may be concluded that the issue of large-scale, *layout-oriented* thermal analysis is still open, although both FEM-based tools [13] or modified Green's function

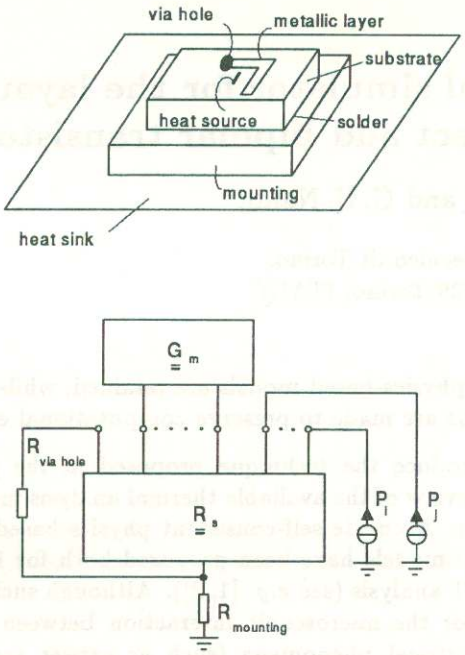

Figure 1: Power device mounting and equivalent thermal network.

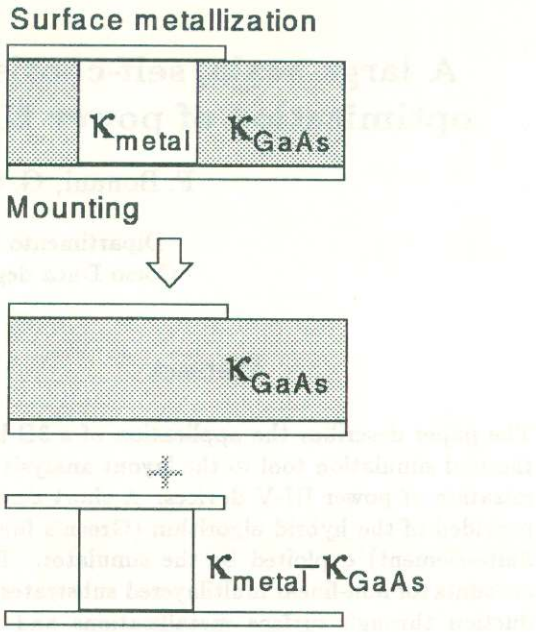

Figure 2: Via hole model based on approximate equivalence principle.

approaches [14] have been proposed to this aim. (Notice that in both cases a non self-consistent heat source is used; moreover, in [14] the treatment of metallizations is approximate only.) In fact, none of the analysis techniques having high accuracy is efficient enough to be exploited as a tool for the layout optimization of realistic III-V devices on a medium-power workstation. Furthermore, it can be remarked that the significance of some model features (*e.g.* including surface metallizations, via holes, or self-consistency of heat sources) and the influence of some parameter models (*e.g.* the substrate thermal conductivity $\kappa(T)$) has not been conclusively assessed.

Analysis technique

The present work proposes a combined approach for the thermal analysis of III-V devices, in which (a) large-scale structures with surface metallizations; (b) multilayered substrates with non-linear dependence of the conductivity from temperature; (c) via-holes and localized substrate thinnings; (d) self-consistency of the heat source distributions, are accounted for. The analysis is based on a hybrid Green's function-FEM approach, whose idea is as follows.

Fig.1 shows an example of power FET or HBT. Metallic layers are deposited on the top surface as the electrical contacts, which may be connected to the mounting through via holes; the position and width of the heat sources is (at least approximately) known [1, 8]. Localized substrate thinnings (ofter referred to as *bathtubs*) can be present; their modelling will be addressed further on. To solve the problem from a numerical standpoint, the upper chip surface is FEM-discretized so as to define the *thermal resistance matrix* of the substrate as $R_{s,ji} = \Delta T_j / P_i$, where ΔT_j is the average temperature increase of element j and P_i is the thermal power injected into element i. $\mathbf{R}_s$ can be computed by means of spectral-domain Green's function techniques or through the method of images [6]. The non-linear conductivity of the multilayered substrate is included through Kirchhoff transformation [15], applied to inhomogeneous regions as discussed in [16]. Finally, a FEM discretization of the top metallizations defines the thermal conductance matrix $\mathbf{G}_m$ of the metallic layers, depending on the metal properties and thickness. The resulting equivalent electrical network is shown in Fig.1. Via holes are approximately included by means of an approximate equivalence principle as suggested in Fig.2. Taking into account substrate thinnigs is less straightforward, since it requires a modification of the substrate Green's function itself. Nevertheless, the problem lends itself to a simplified treatment wherein the self- and mutual substrate conductances are evaluated on the basis of the substrate conductances of the thin and thick substrates. Full details are omitted for brevity and will be presented elsewhere.

The computation includes the following steps: first, the substrate thermal resistance matrix is evaluated; second, the substrate source distribution is evaluated from the network in Fig.1 combined with the Kirchhoff transformation; a self-consistent distribution can be easily recovered through an iterative procedure by means of an approximate electrical model. Notice that the set of nonlinear equations to be solved has a comparatively small dimension (especially if a non-uniform discretiza-

tion has been applied to the metallic layers), equal to the number of nodes (see Fig.1) which either pertain to a metallic layer or to a heat source; in practice, 1000 $\div$ 2000 nodes suffice to simulate realistic devices. Finally, from the substrate heat sources the temperature distribution on the whole device is recovered by use of the substrate Green's function. The computational efficiency is such as to allow the analysis of a large device to be performed in less than 1 hour CPU on a small-power workstation.

Results and discussion

Thermal simulations were carried out on case studies to highlight the influence of different conductivity models, of source self-consistency, and of thick metallic layers (see [18, 17]). While the conductivity model *vs.* temperature may have a dramatic influence on the peak temperature for high-power devices, the effect of metallizations in spreading the heat generated in the active regions, though far from being negligible on the peak temperature, is rather modest on the average device temperature. Source self-consistency is particularly important in HBT devices, where large current densities are present. Comparisons with measured temperature distributions are discussed in [18, 17].

As a first example, a study has been carried out on the layout of a LEP 0.5 μm power MESFET with 20 gate fingers. For an input power of 3.03 W, Fig. 5 shows the distribution of the temperature difference between the conventional layout and a layout with source via holes. Although ΔT is around 5 K on the vias, the cooling effect in the central hot region of the device turns out to be negligible. Fig. 3 shows a section of the device with three different sets of metallizations. This result points out that, in order to achieve significant cooling by means of the heat spred by the electrodes, those have to be unphysically thick (around 20 μm). To the actual thickness (a few μm, 4 μm in the example shown) corresponds a decrease in the peak temperature of the order of 5 K. Thus, it can be concluded that the effect of metallization, though not dramatic, is significant enough on the peak temperature to make their inclusion in the model worthwhile, as already pointed out in [12].

A second case study concerns a power GEC-MACONI 10-finger MESFET. The purpose of the study was to ascertain the impact of a localized substrate thinning, *i.e.* of a bathtub etched below the active region. Fig.6 and Fig.7 show the temperature distribution on the active region for an input power of 1 W with a 50 μm bathtub and without bathtub, respectively. A section of the temperature distribution (across gates) for substrates of different thickness is shown in Fig.4; the effect of substrate thinning in concentrating the heat dissipation under the active region is clearly visible; the peak temperature undergoes a decrease of about 35 K due to

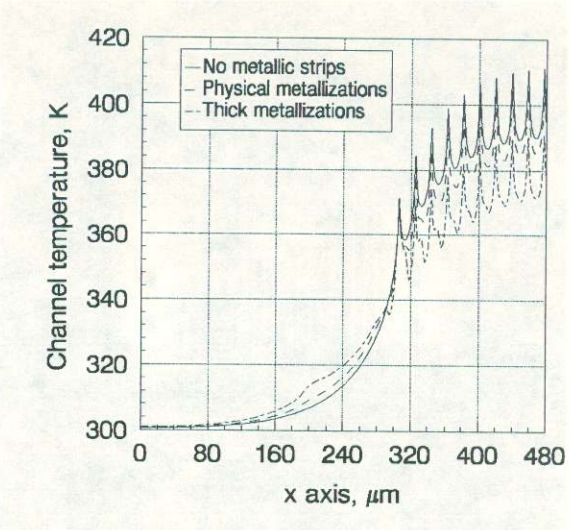

Figure 3: Temperature profile across gates for the LEP FET; only half of the device is shown. The substrate thickness is 100 μm.

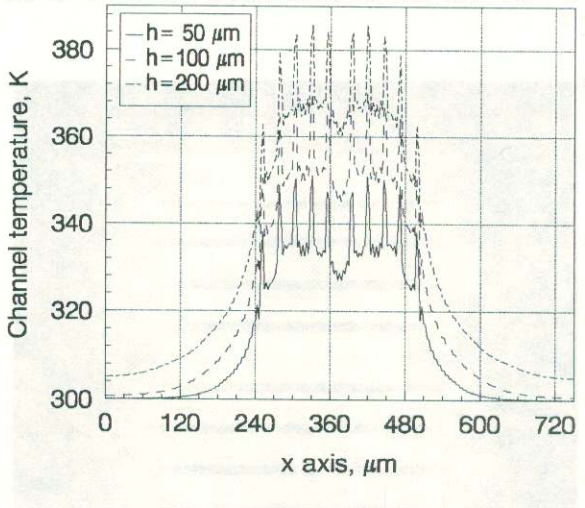

Figure 4: Temperature profile across gates for the GEC FET for different values of the substrate thickness. (The small ripples between temperature maxima are an artifact due to discretization.)

substrate thinning. Since the bathtub drains away most of the heat, the contribution of surface metallic layers and via holes (included in all simulations; the metallization 4 μm thick) is almost negligible.

Conclusion

An efficient and comprehensive large-scale thermal simulation approach for compound semiconductor devices has been presented. The results obtained point out that accurate simulations of the temperature distribution require to account for the effect of heat conduction from metal layers and via holes.

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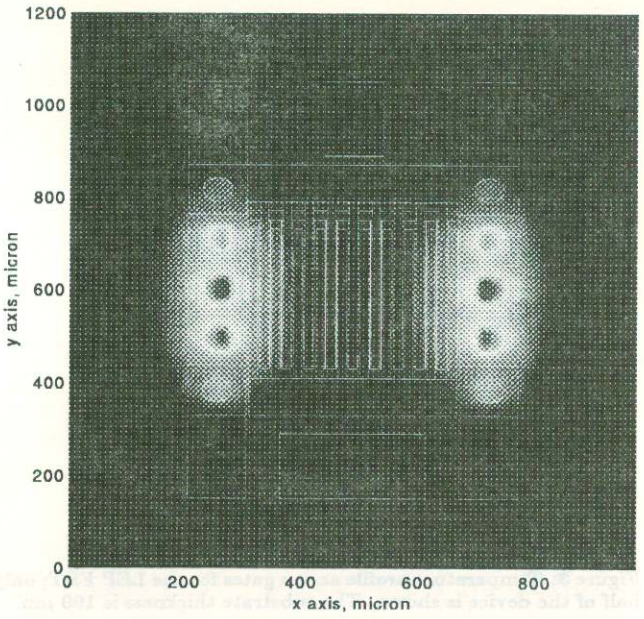

Figure 5: Temperature difference between the device without and with via holes. The maximum difference is 5 K (in the via hole centers).

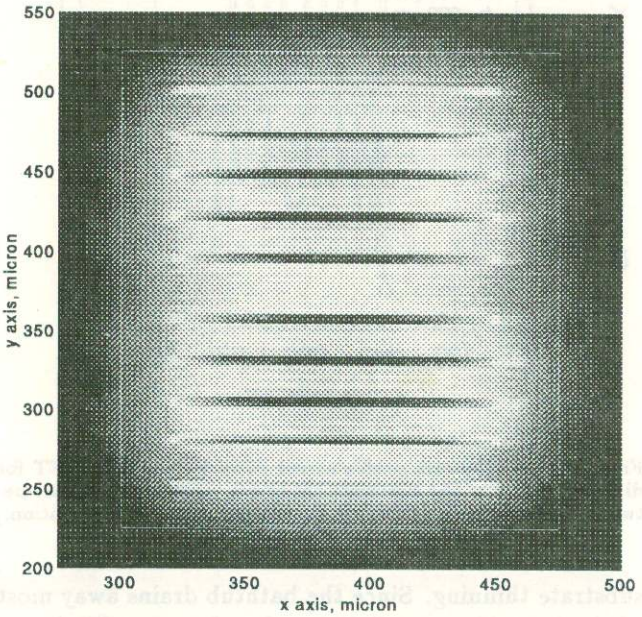

Figure 6: Temperature distribution for the GEC-MARCONI FET with bathtub; the substrate thickness in the bathtub is 50 μm.

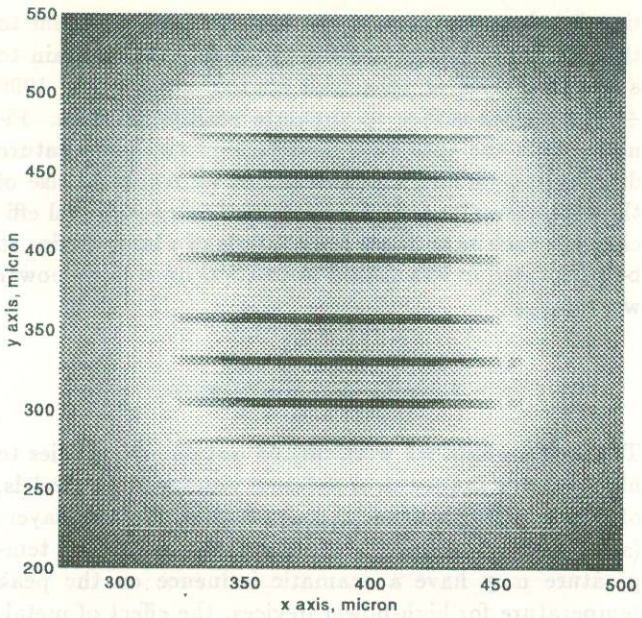

Figure 7: Temperature distribution for the GEC-MARCONI FET without bathtub; the substrate is 200 μm thick.

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