Phenomena description of pulsed characterization of GaAs-MESFET transistors for non-linear modelling purposes

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Abstract

This paper presents a study of the different phenomena that define the large signal behaviour of the GaAs-MESFET as trapping effects and operating point dependence (real heating). These phenomena have been included in a CAD-oriented circuital model. The pulsed measurements have been made maintaining the transistor at each quiescent operating point for several seconds in order to make the operation temperature constant.

Considering the effects described before, a CAD oriented large signal MESFET model capable of simulating DC, pulsed, RF and the I/V characteristic variations with the operating point has been developed. The I_{ds} current is modelled by two non-linear sources, one of them is a bias point dependent nonlinear equation and the other one represents the differences between DC and Pulsed characteristics at every bias point. Experimental pulsed characteristics and simulations, for a 10*140 μm chip transistor from GEC-Marconi foundry, have been carried out, showing excellent agreement. Furthermore, a complete model of this transistor has been obtained. Successful comparisons between MDS simulations using the extracted model and experimental Scattering and power measurements (loaded by 50 Ohms at the input and output ports) have been done. Also, this method has been used to model a 6000 μm chip transistor from PML foundry showing a very good agreement.

Introduction

Several authors [1][2][3] have demonstrated the importance of non-linear characterization of transistors from pulsed I/V measurements. In spite of this, advanced models capable of modelling all phenomena that define the large signal behaviour of the devices do no exist. Therefore, although the designers have powerful software tools to design both hybrid and monolithic circuits, they have important limitations in the development of reliable circuits for civil and military power applications because the foundries cannot supply these advanced models.

Therefore, it is necessary to develop pulsed non-linear models capable of taking into account phenomena such as low frequency dispersion (associated with deep level traps and surface state densities in GaAs-MESFET's [4]), thermal effects and DC, pulsed and RF operation. This means it is very important to describe the influence of these phenomena on the non-linear behaviour of the devices. This study is the main objective of this work, principally oriented to GaAs-MESFET transistor non-linear modelling from drain and gate pulsed characteristics with a CAD-oriented circuit topology. The influence of these phenomena have been demonstrated by simulations and pulsed measurements for a NE720 MESFET transistor.

Following these criteria, an I_{ds} current source model capable of taking into account the operating point dependence (real heating) has been developed. This I_{ds} current equation is principally oriented to GaAs-MESFET transistor non-linear modelling from drain and gate pulsed characteristics. Therefore, along with the DC and scattering behaviour, this equation can predict the different pulsed I/V characteristics at any bias point. Also it is capable of simulating the low frequency dispersion taking into account the real heating of the transistor.

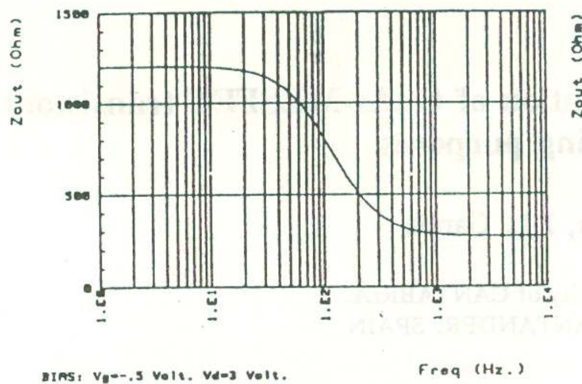
To demonstrate the non-linear behaviour, a complete model of a 10*140 μm GaAs-MESFET chip transistor (from GEC-Marconi Foundry) extracted from experimental DC, pulsed and S parameters along with pulsed breakdown measurements will be presented. Experimental pulsed measurements and MDS simulations permit comparisons between the model from our equation and experimental measurements of the transistor charged by 50 Ohms at the input and output ports, showing good agreement. Also, comparisons between experimental power curves and non-linear simulations using our model for a 6000 μm MESFET transistor from PML foundry have been presented.

Large signal behaviour of GaAs-MESFET's

The different phenomena that define the large signal behaviour of the GaAs-MESFET transistors are:

A. *Trapping effects*

From a macroscopic point of view, these phenomena provoke low frequency dispersion (from DC to some hundreds of KHz) of the transconductance and output



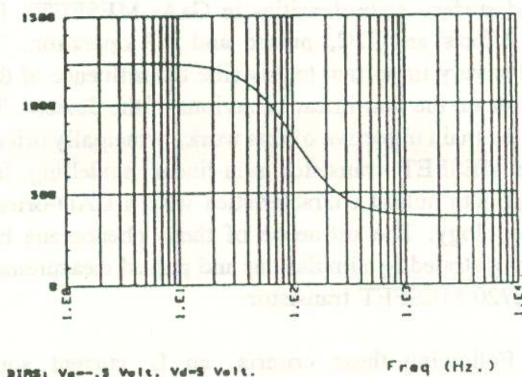


Fig.1 Dispersion of the Real Part of the Output Impedance

conductance [2][4]. In figure 1 we have represented the dispersion of the real part of the output conductance of a packaged NEC transistor at two different operating points.

Taking into account that the pulse rise time, used to obtain the I_{ds} characteristics, is around 50 nS (greater than the cut-off frequency of the low-frequency dispersive phenomena), the influence of these effects in the pulsed characteristics is negligible. Therefore these phenomena have been included in a CAD-oriented circuital model [3].

B. *Operating point dependence*

The variations of the pulsed I/V characteristics with the quiescent point are well known, but it is very important to separate the different phenomena that induce these variations in pulsed operation. From a macroscopic point of view and maintaining the environmental temperature constant, we can distinguish two main effects: One of them is caused by the variation of the average temperature of the transistor at each operating point and the other one is due to the channel resistance variation as a function of gate and drain voltages.

In figure 2 we can observe variations of experimental pulsed characteristics when dissipated DC power does not exist ($V_{dscc}=0$). In this case, we can deduce that the variation of the curves is a direct function of the different channel widths of the transistor. On the other

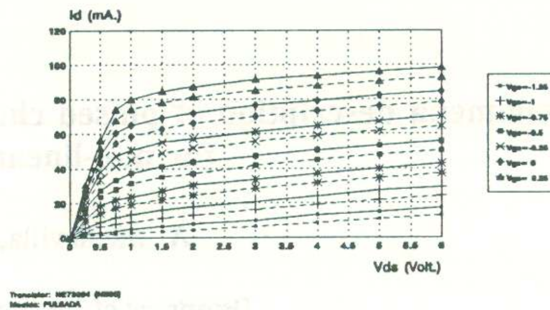


Fig. 2 - Experimental Pulsed Characteristics at $V_{dscc}=0$. Solid lines $V_{gscc}=-.5$, Dotted lines $V_{gscc}=-1$

hand, figure 3 shows pulsed curves for constant DC power at $V_{dscc}\#0$. The variations of the pulsed behaviour of the transistor are provoked by the different channel conditions because the direct dependence between dissipated average DC power and the temperature of the device (different dimensions at the same temperature).

The pulsed measurements have been made maintaining the transistor at each quiescent operating point for several seconds in order to make the operation temperature constant since the thermal time constant of the GaAs-MESFET's is around a few microseconds [5].

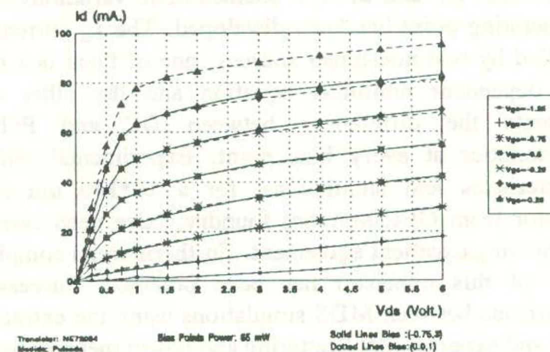


Fig. 3 - Experimental Pulsed Characteristics at $V_{gscc}=-0.75$, $V_{dscc}=3$ (solid lines) and $V_{gscc}=0$, $V_{dscc}=1$ (dotted lines)

Considering the effects described before, a non-linear equation capable of simulating DC, pulsed, RF and the I/V characteristic variations with the operating point has been developed and it will be described in the next section.

Non-linear GaAs-MESFET model

Considering the effects described before, a non-linear equation capable of simulating DC, pulsed, RF and the I/V characteristic variations with the operating point has been developed (Fig. 4). The chosen circuit topology takes into account the low frequency dispersion. The breakdown effect has not been modelled because that is not an objective of this work.

C_{lf} is a linear capacitor and it contributes to simulate the low frequency dispersion. It can be obtained from RF low frequency measurements (From DC to beyond of cut of frequency). Furthermore, C_b and L_b are typical parameters of a low pass filter. These are very important in order to implement the DC dependence in a non-linear simulator and to take into account the variations of the internal bias point (V_{gcci}, V_{dcci}) in large signal RF conditions.

To represent the I_{ds} current, we have develop a non-linear equation function of the internal variables (v_{gi}, v_{di}) and the bias point (V_{gcci}, V_{dcci}). The total equation is given by (1) and (2); as we can see, (1) is based on the Materka equation [6].

$$I_{ds} = I_{dss}\cdot\left[1-\frac{V_{gi}}{V_p+\gamma V_{di}}\right]^{(\mu+\delta V_{di})}\cdot (1+\lambda V_{di})\tanh\left[\frac{\alpha}{I_{dss}}V_{di}\right] \qquad (1)$$

$$I_{dss} = \frac{\beta}{(abs(V_{gcci}-1))^{p}\,(a+V_{dcci})^{q}} \qquad (2)$$

The parameters V_p, γ, β, α and λ are functions of V_{gcci} and V_{dcci}.

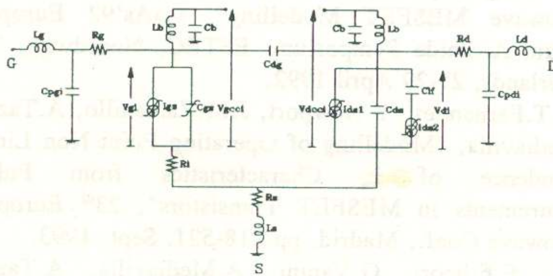


Fig. 4 - Equivalent Non-linear Circuit

Taking into account the circuit of the figure 4, we can write equation (1) as a function of I_{ds1}, I_{ds2}) by:

$$I_{ds}(v_{gi},v_{di},V_{gcci},V_{dcci})=I_{ds1}(v_{gi},v_{di})+I_{ds2}(v_{gi},v_{di},V_{gcci},V_{dcci}) \qquad (3)$$

$I_{ds1}(v_{gi},v_{di})$ represents the DC characteristics of the transistor and it has been modeled using the Materka equation [6]. In figure 5 we can see the experimental and fitted DC curves of a 10*140 μm GaAs-MESFET chip transistor.

$I_{ds2}(v_{gi},v_{di},V_{gcci},V_{dcci})$ takes into account the dependence with the instantaneous voltages (v_{gi},v_{di}) and the internal operating point.

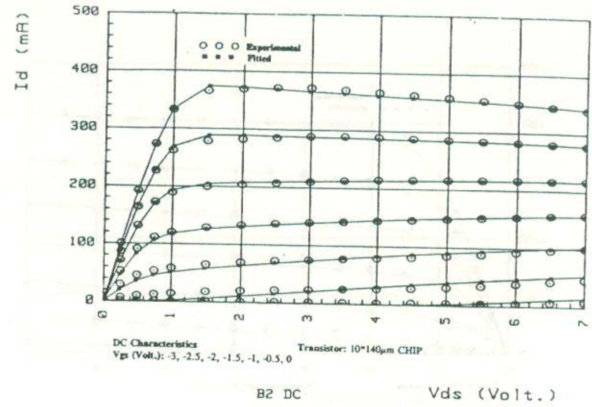


Fig. 5 - Experimental and Fitted DC Characteristics

Simulations and experimental results

To obtain the different parameters of the I_{ds} equation, we need to consider experimental pulsed measurements at five appropriate operating points and to fit the I_{ds} parameters to these key points. The chosen quiescent bias points must follow the V_{gcc} and V_{dcc} gradient. As an example, figure 6 shows the experimental and fitted characteristics at one of the keys points.

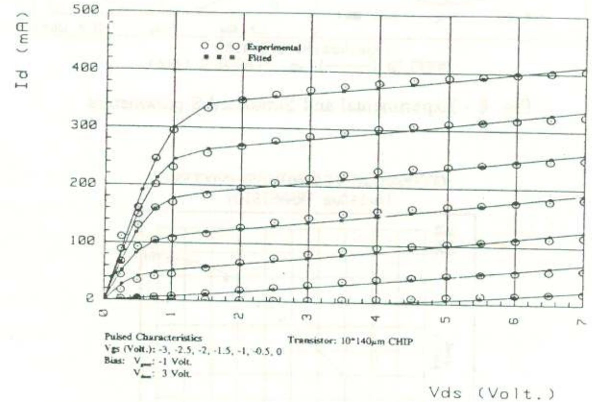


Fig. 6 - Experimental and Fitted Pulsed Characteristics at V_{gscc}=-1 and V_{dscc}=3

The complete extracted model can reproduce the pulsed behaviour of the transistor at any quiescent bias point. Figure 7 shows experimental and reproduced pulsed characteristics at V_{gscc}=-2, V_{dscc}=0.5.

MDS simulations of the total 10*140 μm GaAs-MESFET chip transistor non-linear model permit comparisons between experimental and simulated Scattering parameters (fig. 8) at V_{gscc}=-1, V_{dscc}=3 operating point, as well as, the power behaviour (fig. 9) at V_{gscc}=-1.5, V_{dscc}=3 bias point, being the work frequency 2 (in the case of power calculations) GHz for the same 10*140 μm chip transistor.

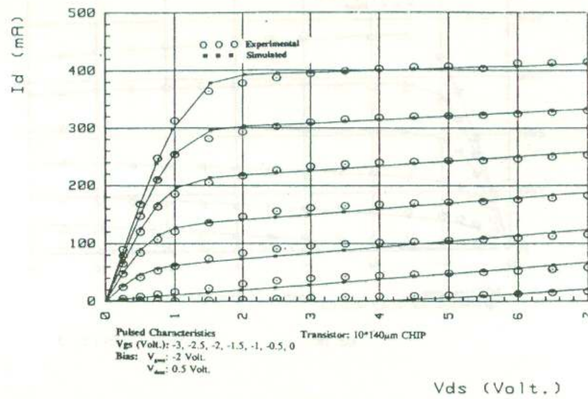


Fig. 7 - Experimental and Simulated Pulsed characteristics at V_{gsoc}=-2 V_{dsoc}=0.5

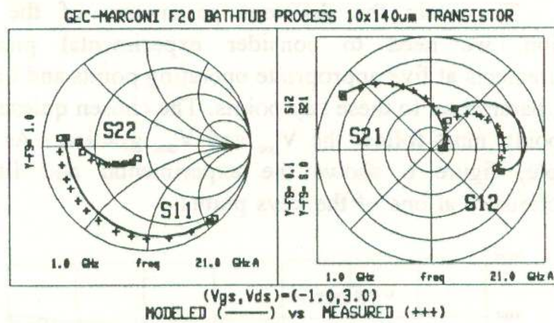


Fig. 8 - Experimental and Simulated S parameters

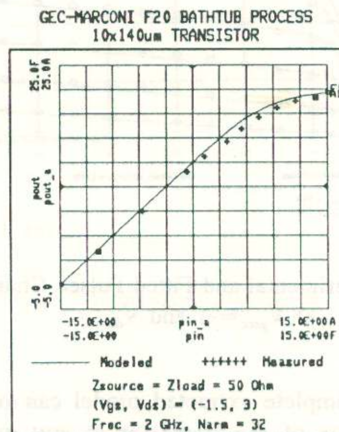


Fig. 9 - Experimental and Simulated Pin/Pout Behaviour

Following the described methodology of non-linear modelling, we have developed a model for a 20*300 μm PML power chip transistor. In figure 10 we can see experimental and simulations Pin/Pout curves showing a good agreement.

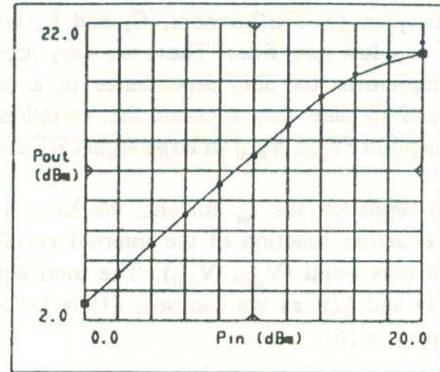


Fig. 10 - Experimental and Simulated Pin/Pout Behaviour for a 20*300μm PML device

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