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ADVANCED CIRCUIT CONCEPTS AND EVOLVING MMIC PROCESSES

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ABSTRACT

This paper discusses the evolution of a typical GaAs MMIC process from its inception to its latest format. Emphasis is placed upon the realisation of circuit design principles driven by the needs of cost and manufacturability **not** just performance although this, of course, cannot usually be sacrificed.

1. INTRODUCTION

Gallium Arsenide MMIC processes and applications are still, frustratingly, considered by many system engineers as "new". This is despite the fact that the basic building block, the GaAs MESFET, was demonstrated in the mid 1960's and the first MMIC processes in the mid 1970's. Commercial supply of MMICs has been underway for nearly 10 years now and, although there has been considerable industry rationalisation, many organisations worldwide now supply commercial parts and services using processes with a similar capability.

Although MMICs are gaining widespread acceptance in a large range of military and civil applications it is worth considering why more customers may have been deterred from using them. There is certainly a view in the user area that GaAs MMIC processes are continually changing i.e. the processes are not stable. This means that a circuit designed one year may no longer be compatible with the technology the next year, causing considerable expense in redesign. Conversely customers tend to be attracted to state-of-the-art capability which is not normally associated with maturity. It is difficult at times to believe that the customer is always right! An attempt is made below to explain how GMMT has tried to handle these conflicting requirements.

2. MMIC FABRICATION TECHNOLOGY

Most manufacturers have processes based upon MESFETs optimised for the frequency range up to ~20GHz. The process described below is the GMMT F20 process which is itself typical of the sophisticated processes from various manufacturers.

In the process schematic of Fig.1 the first-level metal is created at the same mask level as the gate metal, resulting in all the critically dimensioned components being manufactured with the same submicron accuracy techniques inherent in the gate process, with the critical gate itself being 0.5 micron long. This first-level metal (M2) is used for capacitor bottom plates, gates, all underpass interconnections as well as some transmission lines and other passive components. Interlayer dielectrics are then placed on the wafer to separate the metal layers, planarise the wafer surface, provide the overlay capacitor dielectric and to passivate the active devices (Si_3N_4). Via holes are etched through the dielectric layers and filled with metal at those points where connections have to be made between the various metal layers. At this stage a thick, top-level metal (M3) is added which contains the low-loss transmission lines, inductors, capacitor top plates, bond pads and other interconnection features. The front-face wafer processing is then completed by adding a covering dielectric to act as a surface protection/passivation layer.

Once the front-face processing has been completed the IC wafer is then thinned and, if required, through-GaAs via holes are etched before final back-face metallisation and chip separation. Thinning the wafer and backing with metal provides both a ground plane for the microstrip transmission lines and a controlled parasitic image plane for the lumped elements.

The first version of this process entered manufacture in 1985 and differed only in that the gate length was 0.7 microns and no through GaAs vias were included resulting in ~12GHz operation. Circuits designed on that earlier version are still compatible with the latest version. By analogy with software developments the technology is downwards compatible.

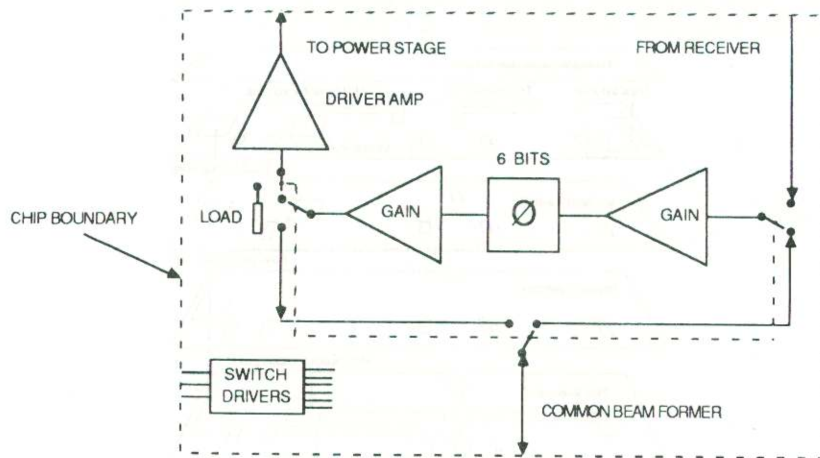

Fig.4a Functional diagram of complex chip

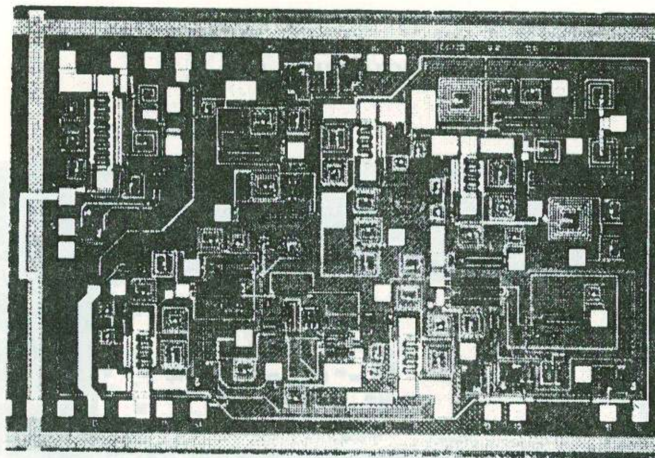

Fig.4b MMIC realisation of function in 4a [Chip area 9.5 sq.mm]

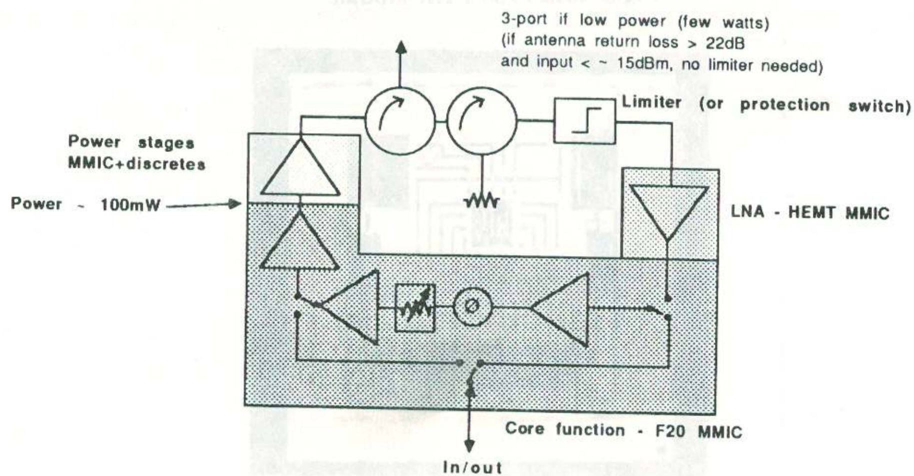

Fig.5 Block diagram of complete T/R Module