GALLIUM ARSENIDE COMPONENTS IN THE EVOLUTION OF ON-BOARD SATELLITE COMMUNICATION EQUIPMENTS

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ABSTRACT

Direct Digital Synthesis technique is fast evolving and is becoming a key point in the design of advanced communication equipments. The growing interest in the use of such a type of technique is strictly related to the increase of speed and bandwidth in the components and the corresponding achievement of attractive performance in terms of frequency resolution and spectral purity.

The increase in the synthesised bandwidth forces the use of very high speed technologies and the use of gallium arsenide devices becomes mandatory to obtain the required performance. The gallium arsenide technology has been playing since many years ago a key role in high-speed analog communication, electronic warfare and analog MMICs but in the recent past has become an astounding weapon also for digital applications. Furthermore processes which combine low-power RF analog and LSI digital functions are now available and they represents a valid alternative to using discrete-components and multichip hybrids for low-power microwave designs.

After a brief review of the DDS concept the paper describes the basic design of the Gallium arsenide numerically controlled oscillator which is the key element of the DDS chain. The experimental results are shown with a particular attention to the spectral purity performance and the modulation capability. The trend of the future on-board applications is given with emphasis on the projects in which Alenia Spazio is presently reusing this specific development.

Keywords: Direct Digital Synthesis, Enhancement/Depletion mode, Gallium Arsenide, Lookup Table, MESFET, Numerically Controlled Oscillator, Source Coupled FET Logic

1. INTRODUCTION

Alenia Spazio is deeply involved in the design and development of advanced equipments for on-board applications making use of a great amount of digital signal processing techniques and state-of-art technologies to achieve attractive performance in terms of size, mass and power requirements. Direct Digital Synthesis represents our last technical achievement in this development line and allows the design and development of a new class of on-board equipments covering a broad range of different applications.

The basic concept of DDS technique is well known and consolidated. A Read Only Memory (Lookup table) stores the sine and/or cosine digitized samples and it is addressed by the digital word coming from the phase accumulator block. The phase accumulator integrates the high clock rate frequency and provides its output to the lookup table. The amplitude samples, which appears on the data bus of the Lookup table, are converted using the output digital-to-analog converter and an output bandpass filter performs the final reconstruction. The phase accumulator block is the key element for DDS operation; it receives an N-bit binary frequency control word which represents the required output frequency and provides the instantaneous phase information.

The accumulator includes registered inputs with delay equalization. A pipeline architecture is used to have a fixed time delay between the input and the output. Frequency modulation can be easily realized changing the phase accumulator content in accordance with the modulating signal, the maximum modulating frequency is about 20 MHz.

The phase modulator block accepts the 11-bit phase control word and two specific input lines (I and Q) for digital modulation schemes. The phase modulator and the phase accumulator outputs are summed and the resulting overall phase information is provided to ROM decoder block for the waveform generation. All types of phase modulation can be realized. Linear modulation is obtained giving as input a phase word proportional to modulating waveform, M-PSK modulation is implemented giving proper words corrsponding to each state in the multilevel modulation. The unbalanced PSK modulation is also possible without any particular complexity, the phase control word must be scaled according to the selected power ratio between the in-phase and the quadrature channel.

The ROM decoder block includes the logic to properly address the look-up table starting from the phase information. In order to reduce the memory dimension only 90 degrees of the sniewave are stored. Two signals, carry on the quadrant and the polarity information, are used to produce the full sinewave. A 12-bit amplitude word is the output for the GaAs DAC to produce the analog waveform. The conversion device is the other key element in the DDS chain. The clock rate of the DAC defines the overall bandwidth and the amplitude quantization has effects on spectral purity as shown in the introduction. A best case figure indicates a spurious suppression of about 6 dB per bit, but glitch pulses, clock feed trough, loading errors and conversion nonlinearities can limit the spectral purity at the output of the DAC.

3. THE TECHNOLOGY

The VLSI technology is the major driving force of the electronics industry and also the space environment has taken great advantage of the advent of very large scale integration. New generation equipments ask continuously for higher density in custom ICs and seek always devices operating at higher frequencies. Charge carriers move faster in GaAs than in silicon, yielding operations three to seven times that of silicon; this advantage can be directly translated to a great improvement in the clock speed for digital GaAs devices. However the much higher speed doesn't mean a direct and proportional higher power consumption. The advent of enhancement/depletion (E/D) mode GaAs ICs increases the speed-power product and make it perfectly tailored for low power applications and large scale integration.

The gallium arsenide technology has played since many years ago a key role in high-speed analog communication, electronic warfare and analog MMICs but in the recent past has become an astounding weapon also for digital applications. Digital GaAs IC was born of microwave TRs technology but digital FETs are different from microwave FETs having as major drivers the low power requirements and the integration scale. The E/D technology has replaced the pure depletion mode as the technology to achieve these specific requirements for digital applications. Furthermore, processes which combine low-power RF analog and LSI digital functions are now available and they represents a valid alternative to using discrete-components and multichip hybrids for low-power microwave designs.

CMOS electrical interfaces have been used for the frequency and phase word input pins, the strobe signals and the I and Q modulation inputs. ECL interfaces have been used for the input clock signal, the amplitude word output and the accumulator MSB output, which gives a square wave at the output synthesised frequency.

The high speed operations of the GaAs ICs force the use of proper packages to support the requirements of high performance ICs. The package is a high-speed multilayer fabricated from cofired alumina ceramic. It provides 84 input/output signal lines, all the signals are carried on 50 ohm transmission lines between the package leads and the cavity bond pads. Ground pins (40) are placed among the signal pins to provide proper signal isolation. In order to have controlled impedance for the signal lines the package consists of several metal layers with ceramic between each pair of metal layers. A proper heat sink allows to handle a power dissipation in the order of 5 watts.

4. EXPERIMENTAL RESULTS

The gallium arsenide numerically controlled oscillator and the digital to analog converter have been integrated and a full characterization of their performances has been performed. The results are very interesting and a sample of them is here presented. Bandwidth and spectral purity are the most important parameters in the DDS technique. Figure 4.1 shows the broadband output spectrum of a 55 MHz synthesised sinewave, a clock frequency of about 260 MHz is used.

In the specific application the DDS chain synthesise a sinewave in the range 52-67 MHz, this plot gives the worst case condition which is very near to theoretical limit. A narrowband plot is shown in fig.4.2. It shows a clear carrier without spurs components. Similar performances have been tested up to output frequencies around 120 MHz. This bandwidth represents the theoretical limit with a 260 MHz clock signal. Using a very simple conversion scheme and a broadband frequency multiplier, the DDS chain can generate S-band and X-band frequencies with a spectral purity better than 50 dBc.

The modulation capabilities are particularly attractive and the test results are hereafter summarized. Fig.4.3 shows a broadband BPSK modulation with 6 Mbit/sec of data rate. The design allows to maximize the spectrum utilization giving the possibility to perform a full digital data shaping. A 3 Ms/sec QPSK signal with digital data shaping is shown in fig.4.4 The phase trajectories are stored in a digital external register and the final phase state is reached in five steps. The result of this process is a shaped signal with fairly constant amplitude envelope and a corresponding sidelobe attenuation. It allows to use non linear power amplifiers (C-class) with a large increase in power efficiency being the sidelobe restoring problem really minimized.

The test results here presented are very encouraging and starting from them a great number of future applications have been identified. The next paragraph gives a generic view of the on-board applications in which Alenia Spazio is reusing the development presented in this paper.

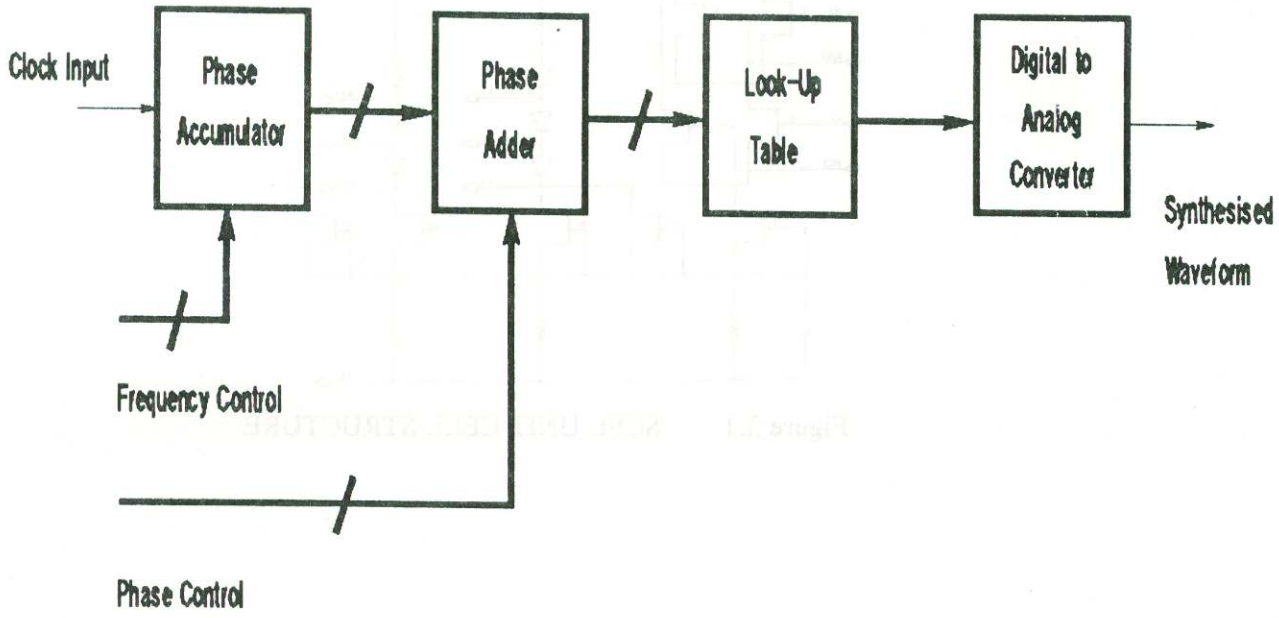

Figure 1 DIRECT DIGITAL SYNTHESIS CONCEPT

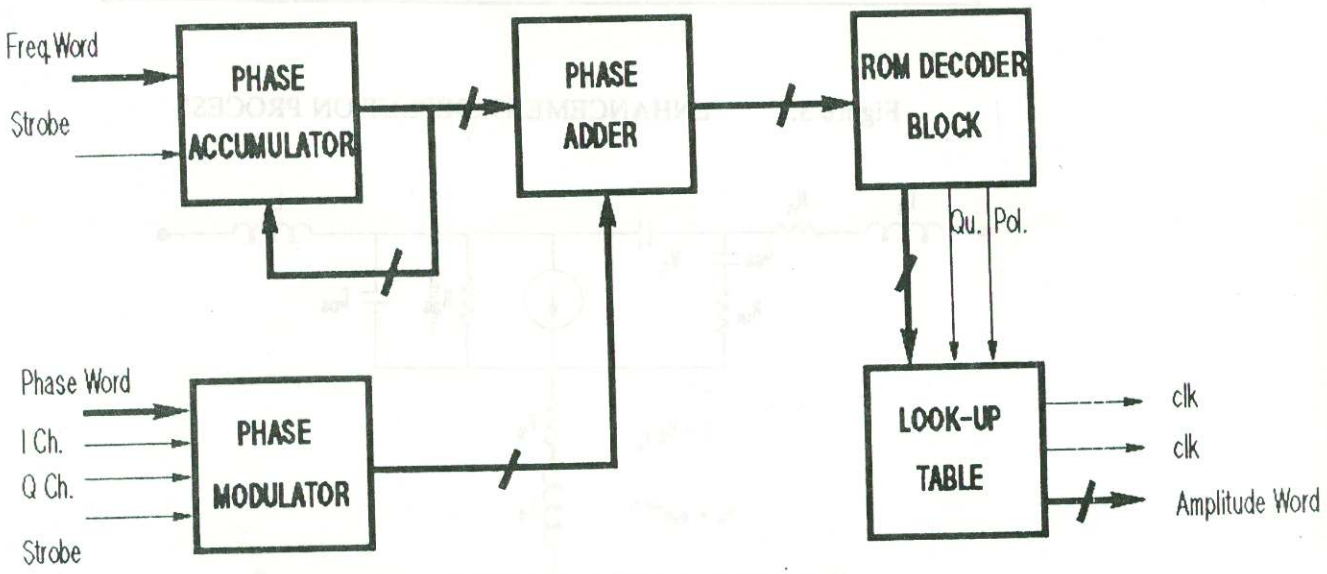

Figure 2 NUMERICALLY CONTROLLED OSCILLATOR BLOCK DIAGRAM

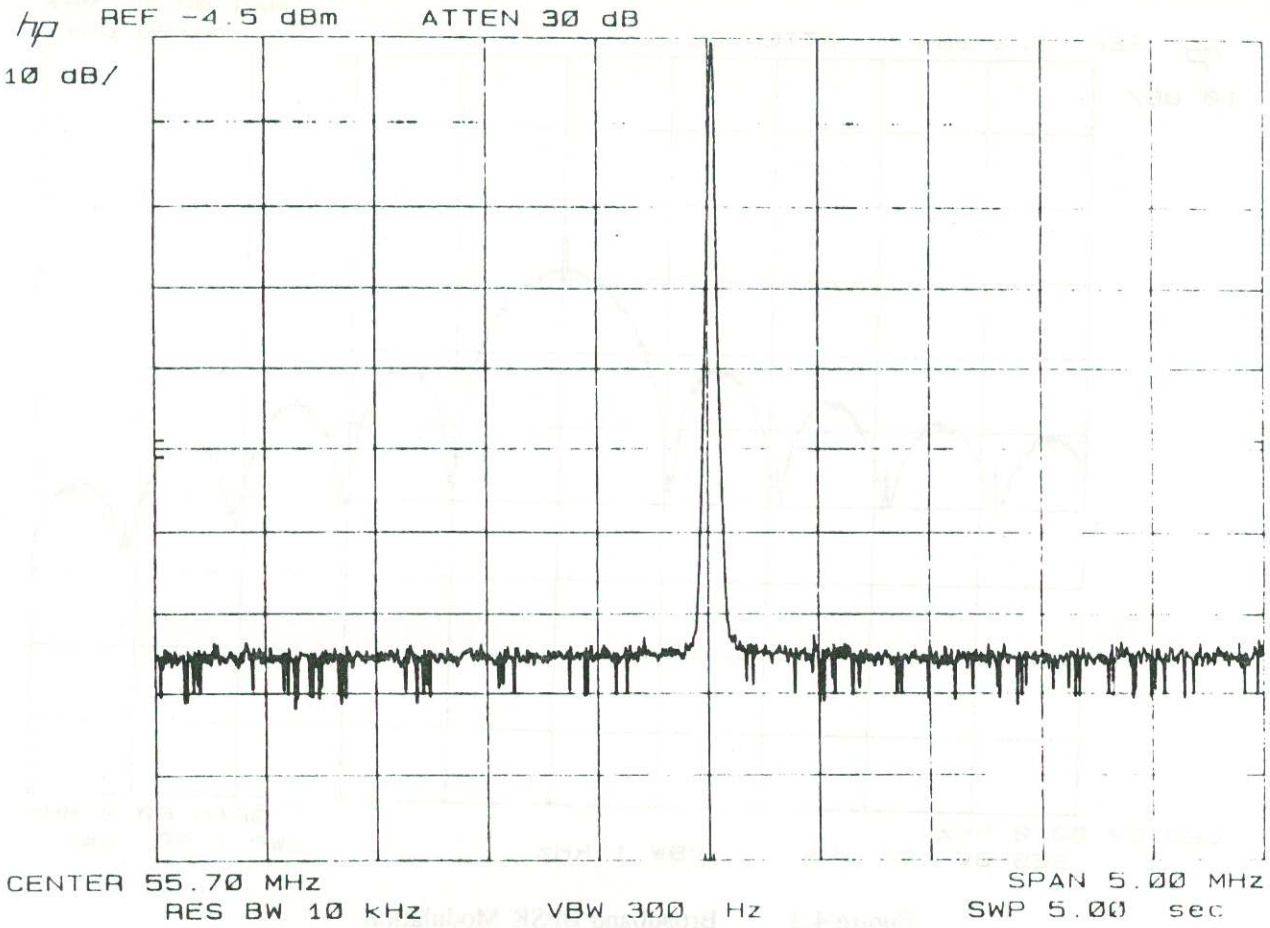

Figure 4.1 Broadband DDS Output Spectrum

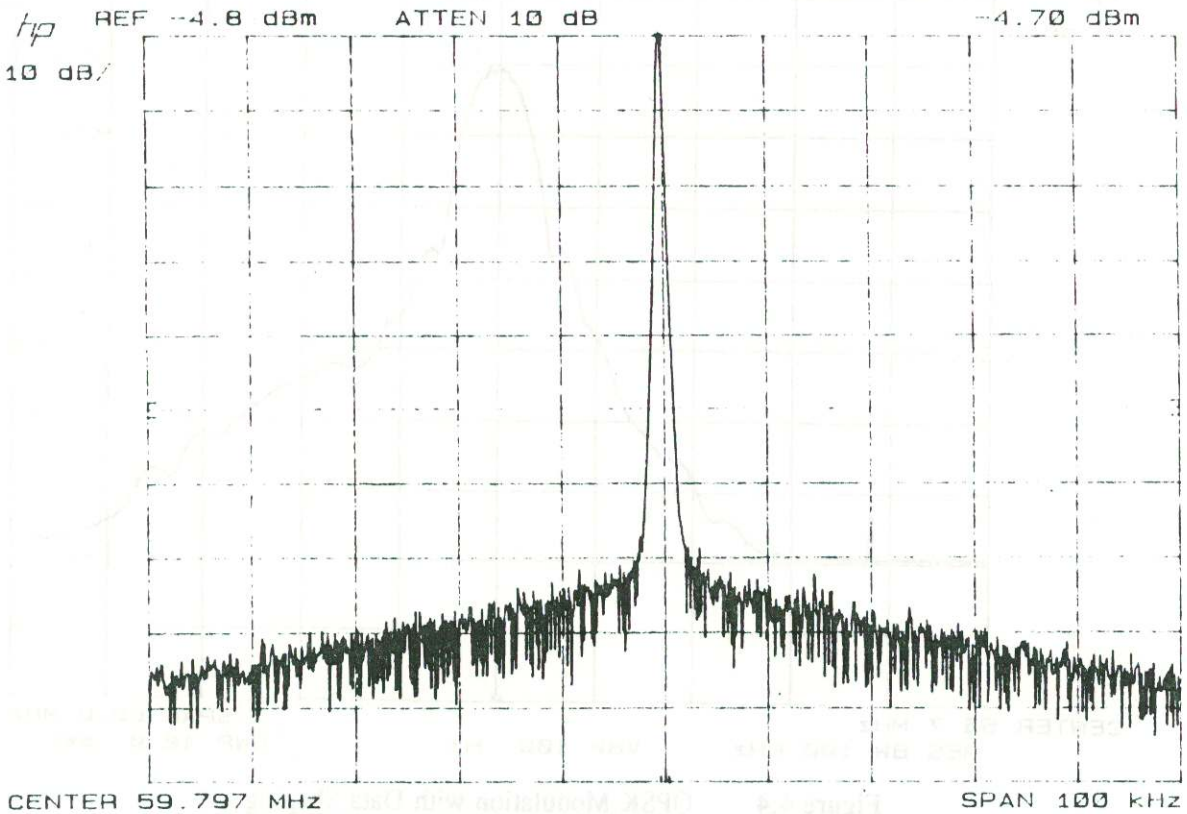

Figure 4.2 Narrowband DDS Output Spectrum

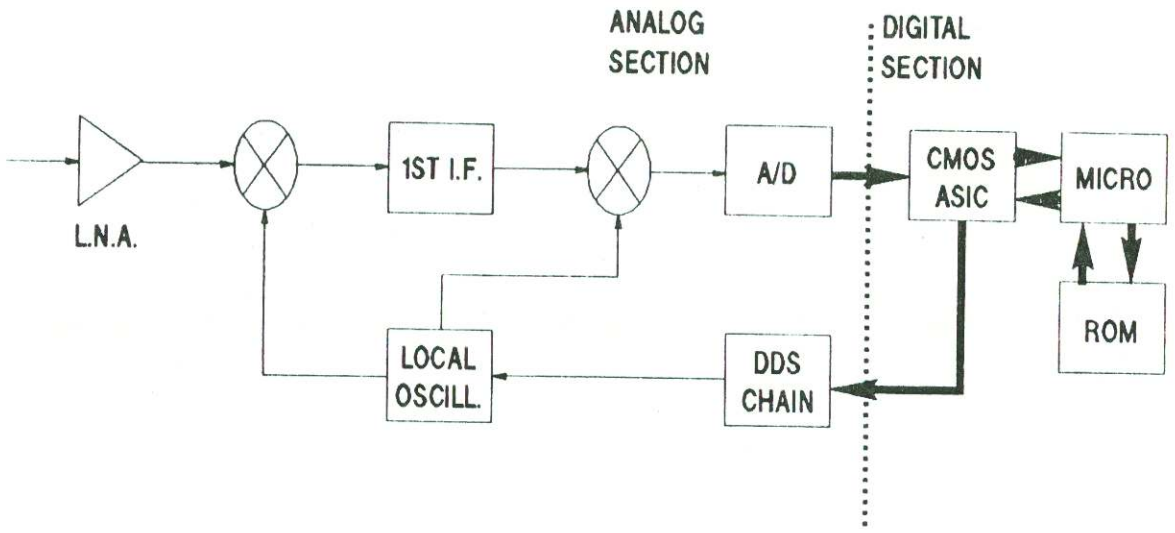

Figure 5.1 FULLY DIGITAL RECEIVER ARCHITECTURE

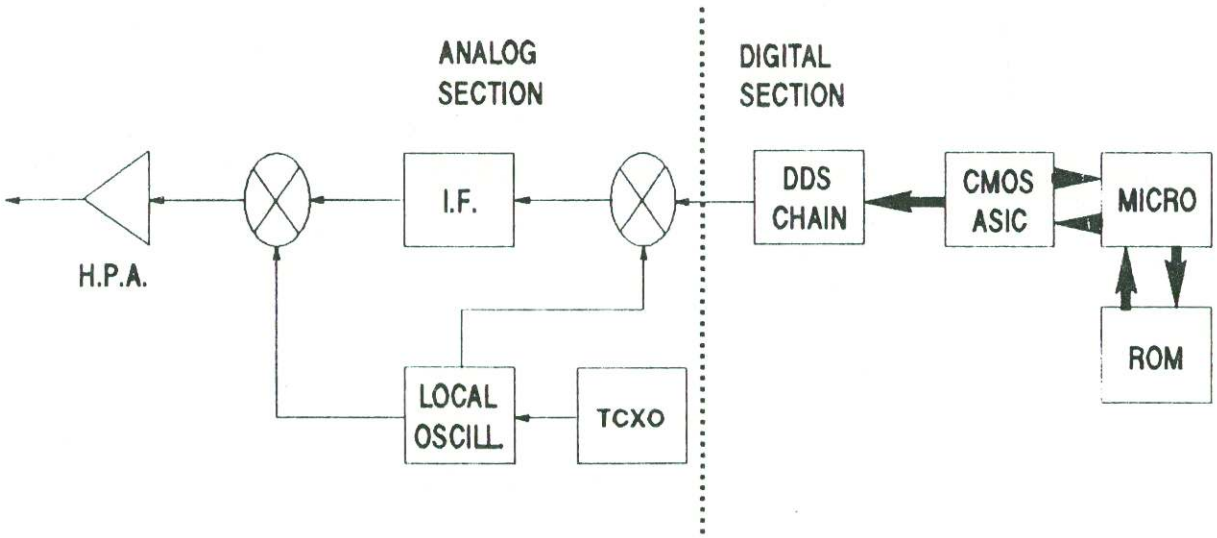

Figure 5.2 DIGITAL TRANSMITTER ARCHITECTURE