TSCFL - A NEW GAAS HIGH-SPEED FAMILY FOR DELAY INSENSITIVE CIRCUITS USING TERNARY LOGIC ELEMENTS

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ABSTRACT

This paper describes a Gallium Arsenide logic family called Ternary Source Coupled Fet Logic (TSCFL) that provides ternary logic elements for use in Delay Insensitive (DI) circuits. These DI circuits are self-timed and operate regardless of delays in wires, logic and register elements. By using ternary levels, only one wire is necessary to implement the necessary coding. The logic elements NOT, OR/AND, EXOR, and a register element have been implemented in TSCFL. A DI FIFO ring test chip was implemented to demonstrate the potential of TSCFL for high-speed DI circuits. Special input circuits were designed to facilitate testing, which take two high-speed binary signals and convert them, on-chip, to a high-speed ternary signal. The test circuits were implemented in the former Gigabit Logic HME/D process, and measurements show TSCFL operation up to 1.5 Gbit/s at a power dissipation of 10 mW/element. The DI FIFO ring runs at approximately 450 Mbit/s.

Keywords: GaAs, Ternary Logic, Delay Insensitivity

1. INTRODUCTION

To date, high-speed digital systems have reached the GHz range in switching speed. Most of these high-speed systems are traditionally designed as synchronous systems. Among the factors limiting the maximum clock rate, the most prominent are: *critical delay path* and *clock skew*. The former requires the global system clock cycle time to be at least the worst case delay path in the system. Problems associated with clock skew are enhanced in high-speed digital systems since propagation times are relatively larger than in low-speed systems. Different strategies can be applied, which do not eliminate but minimize these timing problems in synchronous systems.

Another method of designing digital circuits is to introduce *self-timing* in the system, which eliminates the global clock signal. Such systems operate by self-synchronization through a well defined communication protocol using local *Request* and *Acknowledge* signals.

A special class of self-timed circuits are the *Delay Insensitive (DI) circuits* (Ref. 1). DI circuits operate correctly regardless of delays in wires, logic and register elements. Furthermore, the circuits operate as fast as the technology, implementation, operating conditions and specific input data allow. In DI signaling, the control signals (Request/Acknowledge) are embedded in the data. *Data* values, i.e. *F* and *T* (valid data), are separated by a special value called the empty value, *E* (invalid data). Therefore, a circuit element will alternate between sending *valid data* and *empty data*. This enables the receiving element to detect data transitions. Such a transmission scheme is called four-phase signaling (Ref. 2). The traditional way of implementing the three necessary values is to use *double-rail code* for each data variable (Ref. 3). Double-rail coding requires two wires per logic variable, a false and a true wire. When the signal value on the true (false) wire is high and the signal value on the false (true) wire is low, the two wires together represent a *T* (*F*). A low on both wires represents the empty value, *E*. The last combination of both wires being high simultaneously, is illegal.

Another way to implement DI signaling is by introducing ternary logic elements, i.e. three logic levels. By using the middle level as the empty value, *E*, and the low and high levels as the usual logic values (*F*, *T*), only one wire is necessary to implement the coding. Hence, one of the benefits of using three logic levels on each wire, over two levels on each of two wires, is a 50 percent reduction in interconnection wires.

This paper describes a new GaAs logic family called *Ternary Source Coupled Fet Logic* (*TSCFL*), that provides ternary elements for use in DI circuits. TSCFL is based on the binary SCFL and the Ternary Emitter Coupled Logic (Ref. 4). High speed and good noise immunity are characteristics of TSCFL, which have been inherited from SCFL.

TSCFL is the first completely ternary logic GaAs family, shown to work at high speed (1.5 Gbit/s). A TSCFL DI FIFO ring has been evaluated, which in the author's knowledge, is the first DI circuit to be reported using GaAs. Ref. 5 describes some self-timed circuits in GaAs. In Ref. 6, some attempts were made to develop a ternary logic family based on GaAs, but only a ternary inverter was evaluated at low speeds.

2. THEORY OF DI-CIRCUITS

Delay Insensitive circuits operate correctly regardless of delays caused by wires, logic and register elements. The control signals in delay insensitive signaling are embedded in the input and output data. This requires special elements that take care of the necessary control. In the following subsections, first, the ternary logic and register elements are discussed. Later, the composition of a DI structure using these elements will be described.

register element are synchronized by a C-element and passed to the previous register stage, ensuring that no data is overwritten and thereby lost. Thus, the structure will work, in principle, as the delay insensitive FIFO queue. Notice, that the ternary register element only receives the *status* (*St*) of the succeeding stage, as opposed to the FIFO element in the DI FIFO queue which receives the *output* of the succeeding stage.

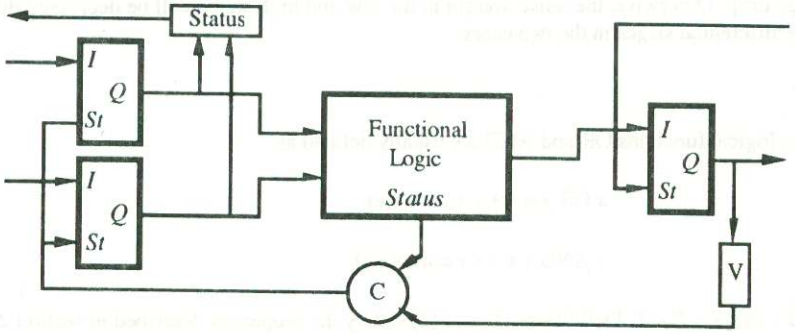

Figure 4: *Ternary delay insensitive structure*

3. TERNARY SOURCE COUPLED FET LOGIC (TSCFL)

TSCFL is based on the binary SCFL, and like the Ternary Emitter Coupled Logic elements, the ternary logic function is implemented using an additional current source. In the following subsections the basic operation of TSCFL, the logical elements and finally the register element are described.

3.1 Theory of operation

Figure 5 illustrates the basic TSCFL inverter (NOT) circuit, which consists of two level shifters and two differential amplifiers. TSCFL is fully differential with input terminals at the level shifters, and output terminals at the resistors. When valid data (*F* or *T*) is applied to the input terminals, the function of the ternary inverter is the same as that of its binary counterpart. When the input data (*E*) is invalid, the output also produces invalid data. Thus, the inverter satisfies the requirements for a ternary element. Since *NI*=NOT(*I*), the inverter as a logic element is superfluous, although it might be used as a buffer. The voltage levels representing the three logical values are

T	:	$V_{Q,HIGH}$	=	0 (ground)
E	:	$V_{Q,MIDDLE}$	=	$-R \cdot I_{cs}$
F	:	$V_{Q,LOW}$	=	$-2R \cdot I_{cs}$

Figure 6 illustrates the operation of the inverter. When *I* is high (*NI* low), transistors T_1 and T_3 conduct, while transistors T_2 and T_4 are cut off. This implies the potential at node *Q* to be $-2R \cdot I_{cs}$, which represents a low. At the same time, the potential at node *NQ* is equal to ground (i.e. high). When *I* is equal to the middle value, T_4 is switched on and T_3 is switched off. T_1 and T_2 remain on and off respectively. This implies that both outputs are $R \cdot I_{cs}$ below ground, which by definition is the middle value. Finally, when *I* equals low (*NI* high), T_2 and T_4 are on, and both T_1 and T_3 are off. The potential at node *Q* increases to ground (high). Simultaneously, the potential at node *NQ* drops to $-2R \cdot I_{cs}$ (low).

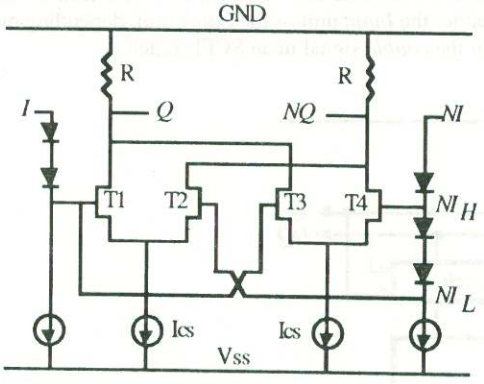

Figure 5: *TSCFL NOT*

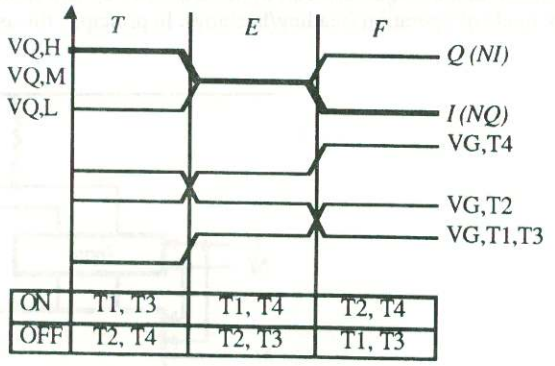

Figure 6: *Basic operation of TSCFL*

Note, that TSCFL in principle operates as its binary counterpart (SCFL). This implies that design techniques used for SCFL (Ref.7) can be applied to TSCFL. For proper operation, the diode voltage drop should be large enough to completely switch a differential pair of transistors (see Figure 5 with *I* and *NI* equal to middle) with some safe margin allowed to account for

4. IC FABRICATION

Test circuits containing TSCFL NOT, OR, EXOR and a delay insensitive FIFO ring were fabricated in the former Gigabit Logic HME/D process (0.8 µm E/D-MESFET). Open drain output buffers capable of driving 50 Ohm lines were used on all high-speed outputs. Due to the lack of ternary test signals, a special input circuit was designed which generates a high-speed ternary signal from two high-speed binary signals. All measurements were done on-wafer using a Cascade Microwave probe station. All circuits were designed to operate at Vss equal to -6 Volts, with logic levels of 0V (*T*), -0.7V (*E*) and -1.4V (*F*).

4.1 Results

Figure 9 shows the transfer characteristics of a TSCFL inverter. It appears that the noise margin in all the three states are approximately the same. The power dissipation was 8mW. Figure 10 shows a similar TSCFL inverter operating at 1Gbit/s. (*1 bit* is equivalent to one valid data value plus one empty value). The maximum speed of operation was measured to be approximately 1.5 Gbit/s.

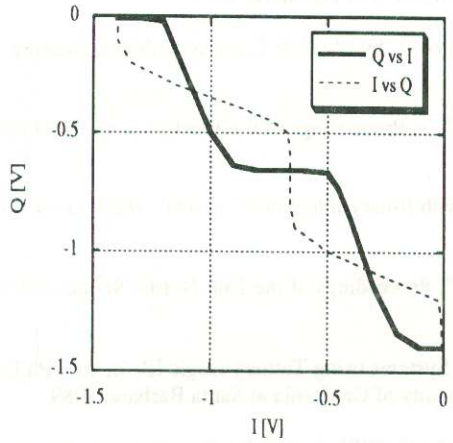

Figure 9: *TSCFL inverter transfer characteristic*

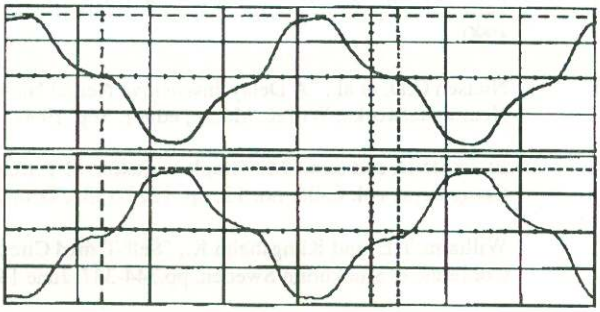

Figure 10: *TSCFL inverter operating at 1 Gbit/s. Differential outputs. 500 ps/div, 400mV/div*

To demonstrate the potential of TSCFL for high-speed DI circuits, a DI FIFO iterative ring was implemented. It consists of three register elements and three validity detectors (see Figure 11). The dashed inverter indicates that the differential wires are interchanged in this interconnection. By this arrangement, the valid data value rotating in the ring will be *T* and *F* alternately. To ensure that the FIFO ring would start up in a well-defined state, i.e. a state which satisfies the delay insensitive signaling (each valid data value must be separated by at least one empty), an *Init* signal was used (not depicted). Once initialized, the FIFO ring behaves as the DI FIFO queue described in section 2.3, and measurements have shown an operating speed of approximately 450 Mbit/s (see Figure 12). The total power dissipation was 370 mW, with the output driver accounting for approximately 300 mW. Lowering the power supply by 10 percent slows down the operating speed (420 Mbit/s) of the DI ring. However, because it is a DI circuit, it still functions correctly.

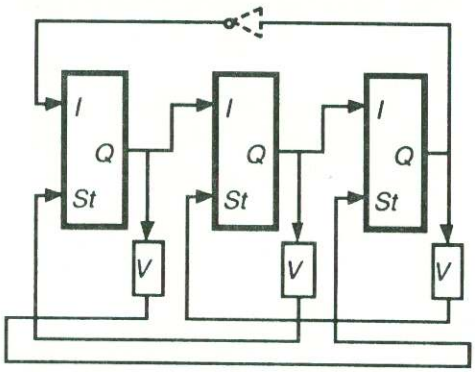

Figure 11: *TSCFL DI FIFO ring*

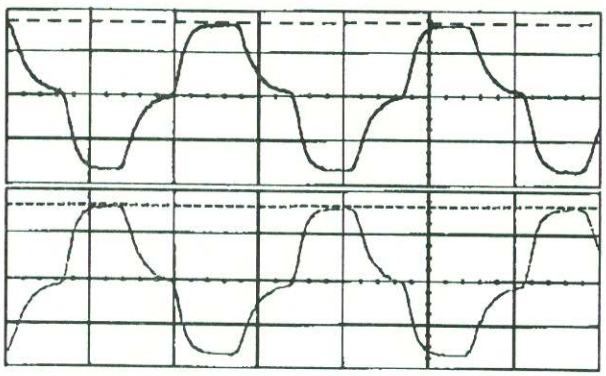

Figure 12: *TSCFL DI FIFO ring operating at 450 Mbit/s. Differential outputs. 5.0 ns/div, 400 mV/div*