2^{15}-1 PSEUDO RANDOM BINARY SEQUENCE TRANSMITTER AND RECEIVER CHIP

Niels Thybo Johansen*, Per Danielsen, Jesper Riishøj and Peter Lassen

Center for Broadband Telecommunications
Electromagnetics Institute
Technical University of Denmark
DK 2800 Lyngby, Denmark

ABSTRACT

This paper presents the design and test of a transmit/receive Pseudo Random Binary Sequence GaAs chip. The chip is designed using a parameterized Source Coupled FET Logic library. The chip can deliver sequences of length 2^7-1 and 2^{15}-1 at bit-rates up to 2.2 Gbit/s.

1. INTRODUCTION

To test digital communication systems CCITT recommends the use of PRBS (Pseudo Random Binary Sequences). A PRBS sequence can be generated using a series of D-FlipFlops and a number of XOR-gates. One of the acceptance criterias for communication systems under development today is a Bit Error Rate (BER) of less than 10^{-9} at a transmission rate of 2.5 Gbit/s.

Today, commercial PRBS-generators are available up to 15 Gbit/s. The price is fairly high, since the high speed circuits are build using discrete components. To avoid this problem the aim of this work has been to investigate what complexity could be achieved on a single GaAs chip. The chip was designed employing the 0.8 µm gate-length HMED process of GigaBit Logic. To minimize the power consumption and to increase the maximum speed it has been necessary to develop a parameterized standard cell library containing different FlipFlops and a number of discrete gates. A further advantage appears in the layout phase, where the cells are adjusted in size, so they can be placed in a long row. It minimizes the area requirements as well as the wiring capacitance, since no routing channel is needed.

2. LOGIC DESIGN

The basic structure of a PRBS-generator consists of a series of D-FlipFlops looped back by one or more XOR-gates (Ref. 1,2) using the approach shown in Figure 1. It can be proved, that if the number of D-FlipFlops is m, then a sequence of length $n=2^{m-1}$ can be generated by proper insertion of XOR-gates in a loop-back (Ref. 1-2). For the measurement of the BER CCITT recommends the following values of m: 7, 9, 15, 22 and 31. The selector SE1 in Figure 1 can switch between polynomials of order m=7 and m=15. The shift register can be set in a well-defined state by setting the Reset pin.

In Figure 1 the critical path is shown as a bold line. The maximum speed is determined by the propagation delay in the XOR-gate and a FlipFlop. To increase the bit-rate and to decrease the power consumption an other solution was chosen, where the chain of D-FlipFlops is running at half speed (Ref. 3). Two different signals in the chain are multiplexed together and a bit-stream at the double bit-rate is obtained. This scheme has been applied in Figure 2, where a multiplexer has been inserted. The selector SE1 has now been replaced by two selectors.

---

* Now with Oilcom.

For analysis of the transmitted data, identical data sequences have to be generated at both the transmitter and receiver to allow a bit-by-bit comparison. The difficulty in implementing such a scheme lies in the synchronization of the locally generated reference pattern with the received sequence. A solution to this problem is the Westcott-receiver (Ref. 4), which contains a shift-register chain, that is identical to the transmitter, but where the feedback-loop is left open. The maximum bit-rate of this solution is however limited by the critical path in the shift registers.

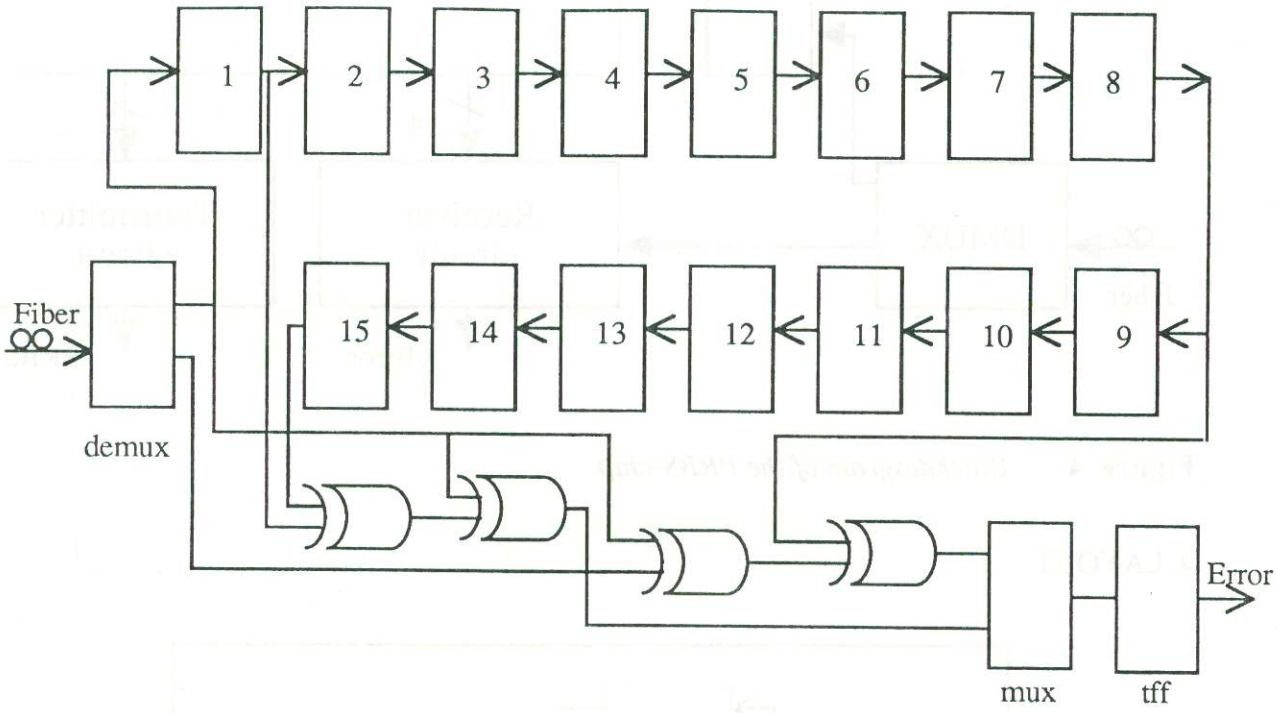

Figure 3 *Modified Westcott-receiver.*

It is possible to increase the input bit-rate by applying our newly developed Modified Westcott-receiver. This receiver makes use of multiplexing, whereby the maximum input bit-rate is doubled without increasing the circuit complexity considerably, see Figure 3.

The final chip has been partitioned into three blocks: A common circuit for both the transmitter and receiver part, a dedicated receiver circuit and a dedicated transmitter circuit, see Figure 4. The partitioning also makes it possible to reduce the power dissipation on the chip, because the transmitter dedicated circuits can be switched off, when the PRBS-chip is used as a receiver and vice versa

3. SIMULATIONS

The correct function of the chip was first verified using the Mentor Graphics digital simulator Quicksim. Next, the individual cells were designed using Source Coupled FET Logic (SCFL) to obtain high speed and large noise margins. In each cell the gate widths were scaled to obtain a load independent current gradient in time. The load is implemented as a diode clamped active load, which reduces the influence of the process variations on the logic levels. The design of the cells was verified through SPICE simulations of the individual cells and of the whole chip (Ref. 5).

parts. The cells are constructed in a number of discrete sizes to account for the variable load. The outer dimensions of the cells are adjusted to facilitate a connection by abutment of the clock and power lines. This minimizes the need for routing channels.

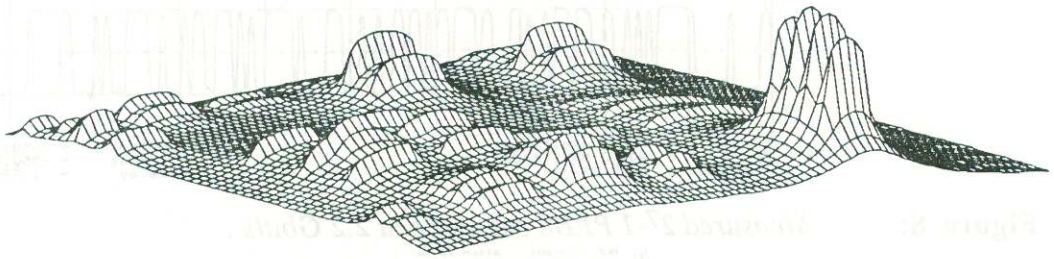

Figure 6: *Temperature variation on the chip*

The temperature variation on the chip has been simulated by considering the MESFETs as thermal line-sources. The temperature variation for the whole chip is shown in Figure 6. The maximum temperature is achieved in the in- and output-buffers, where the temperature is about 100 °C. For the rest of the chip the temperature is about 70 °C. This will secure a reasonable lifetime for the chip (Ref. 6).

5. MEASUREMENTS

The chip functions up to a bit-rate of 2.2 Gbit/s for both sequences. Figure 7 shows a part of the PRBS sequence at 2.2 Gbit/s and Figure 8 shows a complete 2^7-1 sequence at 2.2 Gbit/s. The 2^7-1 sequence is in full agreement with a Quicksim simulation. An other proof of the function can be obtained from the power spectrum. Figure 9 shows the measured power spectrum for the 2^7-1 sequence at 2 Gbit/s. The peaks are all placed equidistant, which proves that the sequence is a true PRBS sequence. A similar spectrum is obtained for the 2^{15}-1 sequence. The power consumption is 4.7 W and the output swing is 0.8 Volt. The measured rise and fall times for the individual bits are given in Table 1.

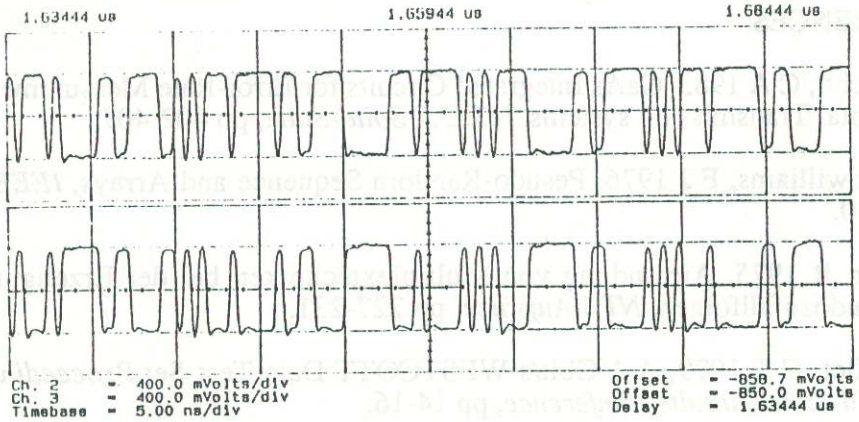

Figure 7: *Measured 2^{15}-1 PRBS sequence at 2.2 Gbit/s*

	20-80 %	10-90 %
rise time	96 ps	160 ps
fall time	84 ps	136 ps

Table 1: *Measured rise and fall times*

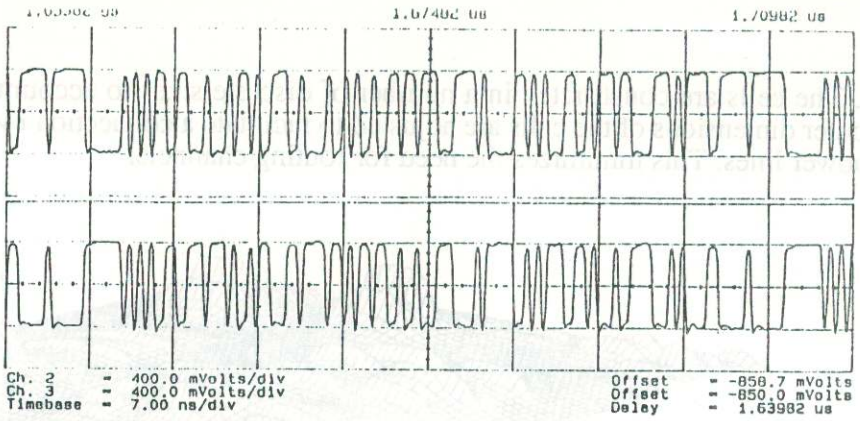

Figure 8: *Measured 2^7-1 PRBS sequence at 2.2 Gbit/s .*

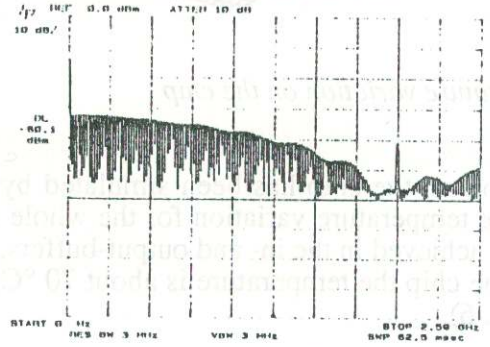

Figure 9: *Measured power spectrum for a 2^{15}-1 PRBS sequence at 2.2 Gbit/s*

6. CONCLUSION

In conclusion we have developed a fully integrated PRBS-chip in SCFL. The chip occupies 1.8*3.6 mm^2 containing 859 MESFETs and 737 diodes. The measured maximum bit-rate is 2.2 Gbit/s for both 2^7-1 and 2^{15}-1 sequences at an output voltage of 0.8 Volt. The power dissipation is 4.7 W. The measured rise- and fall-times (20-80 %) for the output signals are less than 100 ps.

7 REFERENCES

1. Liechti, C A 1983, GaAs Integrated Circuits for Error-Rate Measurements in High Speed Digital Transmission systems, *IEEE J. Solid-State*, pp 402-407.

2. Macwilliams, F J 1976, Pesudo-Random Sequence and Arrays, *IEEE Proc.*, pp 1715-1730.

3. Eier, R 1975, Anvendung von Multiplextechniken bei der Erzeugung von schnellen Pseudozufallfolgen, *NTZ-Aufsätze*, pp 227-231.

4. Mallet, C T 1979, A 1 Gbit/s WESTCOTT Data Test Set,*Proceedings 5th European Solid-State Circuits Conference*, pp 14-16.

5. Johansen N T, Danielsen P, Riishøj J and Lassen P 1991, New Design Methodology for GaAs PRBS Chips, *Proceedings Sixt Norsilc/Norchip Seminar*, pp 17.0-17.9.

6. Kraus D A and Bar-Cohen 1983, *Thermal Analysis and Control of Electronic Equipment*, McGraw Hill.