# A 3V SMALL CHIP SIZE GSM HBT POWER MMIC WITH 56% PAE

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## ABSTRACT

A three stage 56% power added efficiency (PAE) InGaP/GaAs HBT power MMIC for use in GSM applications (900MHz) is described. An output power of 2.7W is obtained at the connectors of the evaluation board with a single supply voltage of 3.2V. The large signal gain is in excess of 32dB and the dynamic range for power control exceeds 80 dB. The chip size of only 2mm² allows housing in a tiny plastic package (TSSOP10) which occupies less than one half of the board area compared to packaged GSM devices before.
For circuit design an accurate electrothermal large-signal HBT model is used. For characterisation of large emitter area power transistors on-wafer large signal measurement techniques have been developed which assist model verification and provide new insights in the influence of harmonic load terminations. The design techniques employs two steps. In a first step on-wafer loadpull measurements provide reasonable conditions for output power, which are combined with appropriate small-signal simulations to fix the circuit topology in principal. In a second step refinements of the power performance are achieved by large-signal simulations.

## INTRODUCTION

In handheld telephones power amplifiers are key parts which influence important system parameters like talktime, size, and overall cost. GaAs MESFETs offer acceptable 3V performance at low chip cost. However, they normally require two voltage supplies (both positive and negative) for operation and a drain supply switch for low drain currents in the standby mode. The additional circuitry increases cost and board area. These disadvantages are circumvented by devices like Si-LDMOS, Si Bipolar and GaAs HBT, which allow unipolar operations. The drawback of Si technologies is that for the application in mind a power device is required which combines good large signal performance at low voltage operation and high breakdown voltages. (Amplitudes of 15V may occur at the amplifier output if the phone is used when charging the batteries).
GaAs HBTs offer an attractive solution to this problem. The use of GaAs in general offers low parasitics due to the semi-insulating substrate and high mobility and velocity of carriers. High Q passive elements for matching are available. Substrate vias can be processed for low inductance ground connection, offering small chip sizes and use of small packages with low lead count. High frequency performance combined with high breakdown voltage is achievable, even with relaxed 3µm lithography.

## DEVICE PROCESSING

The power HBT MMICs were fabricated using our 4“ production line for GaAs MESFETs due to the high degree of compatibility of both processes. 4 inch-diameter MOCVD grown wafers were non self-aligned processed using i-line stepper photolithography. The epitaxial layer sequence mainly consists of a N-InGaP ($4x10^{17}$ $cm^{-3}$) emitter layer, a p-GaAs ($4x10^{19}cm^{-3}$) constant doped base layer, a 700nm n-GaAs ($2x10^{16}cm^{-3}$ ) collector and a 700nm thick n-GaAs ($5x10^{18}cm^{-3}$ ) subcollector layer. Dopants for the n- and p-type layers are Si und C, respectively. The HBT process shows following features:

- Non-alloyed metallisations for emitter (WSi/Ti/Pt/Au) and base (Pt/Ti/Pt/Au) contact formation.
- Selective etch stops during dry etching to improve process control and device homogeneity across the wafer.
- Metal-isolator-metal (MIM) capacitors, electroplated airbridge metallization, wafer thinning and backside via holes.
- The multi-emitter cells are composed of 3x45 $\mu m^2$ one-emitter-fingers with 32µm spacing, which allows for a compact power cell design. The emitter airbridges serve as a thermal shunt [1, 2] by spreading the heat over the chip and contributing to a more uniform distribution of temperature between fingers.

The favourable characteristics of the HBT process summarised in Table 1 allow achievement of high values of output power and efficiency for low bias voltage operation in the wireless frequency bands.

## HBT MODELLING

One of the major challenges when designing HBT power MMICs is careful thermal management [2] to prevent hot spot formation in the large emitter area power stages as well as accurate description of their electrical characteristics. For this

purpose an electro-thermal large signal model of the HBT has been developed, which allows scaling of the HBT emitter area (Fig. 1). The model allows an accurate simulation of the DC-characteristics [3] of the HBT by considering the ambient temperature and the effect of self-heating. For this purpose an equivalent thermal circuit is used, which consists of the thermal resistance $R_{th}$ of the device, the current source $P_{diss}$ , whose current is proportional to the dissipated power, and the thermal capacitance $C_{th}$. The increase of the junction temperature $\Delta T$ equals the voltage drop across $R_{th}$. $R_{th}$ can be determined by simple measurements of the DC output characteristics of the HBT at two substrate temperatures [4].

## ON-WAFER CHARACTERISATION OF LARGE EMITTER AREA POWER HBTs

For evaluation of the performance of large emitter area power transistors on-wafer large signal measurement techniques have been developed, which include static IV-output characteristics for currents up to 5A, pulsed IV-output characteristics for currents up to 10A, static and pulsed S-parameter measurements in those current ranges, active harmonic loadpull [5] measurements up to 10W. Thus, after finishing front-side processing the quality of the wafers in respect to their power performance can be judged, which helps to speed-up process optimisation. Fig. 2 shows pulsed IV-measurements of the output characteristics ($I_c$ up to 4A) of transistors with emitter areas of 1440, 4320 and 8640µm², normalized to $I_C$ of the largest cell. The pulse conditions were adjusted according to GSM requirements ($T_{on}$=0.58ms). The currents of the large emitter area HBTs scale accurately with emitter area demonstrating that their process and layout have been successfully optimised.
Fig. 3 represents the on-wafer measured maximum available gain MAG (respectively, the maximum stable gain MSG if k<1) as a function of frequency for HBTs with an emitter area of 4320µm² ($V_{CE}$=3.2V, $I_C$=432mA). Here, the results of ten HBTs selected from different locations across a wafer are shown. The small variations demonstrate good homogeneity of RF-gain across a wafer for the large emitter area power HBTs. In addition, at 900MHz high values of MSG≈25dB have been obtained.
Figs. 4 to 6 show the outcome of on-wafer loadpull measurements again for an HBT with an emitter area of 4320µm², operated at a very low quiescent current $I_Q$=43mA at 3.1V. The load and biasing conditions were adjusted to near class-B operation and the influence of fundamental and harmonic load conditions studied at 900MHz. For Figs. 4 and 5 the load at the fundamental frequency was adjusted to give a good compromise for high values of output power $P_{out}$, gain and power added efficiency PAE. The loads of the second up to the fifth harmonic were chosen to 50Ω. Mainly due to the very low quiescent collector current, the gain is approximately 7dB less compared to the result from Fig. 3, but shows still values in excess of 17.5dB. Fig. 4 represents a power sweep of $P_{out}$ , PAE and $I_c$ versus $P_{in}$ . High values of output power (31.5dB) and PAE (56%) have been obtained. Note that due to self-biasing the collector current increases to 800mA for maximum output power. For comparison the simulated performances are also shown. The good agreement between measurements and calculations confirm the accuracy of the HBT model.
Fig. 5 shows a power sweep of the harmonic content. For the input power where maximum PAE occurs, the third harmonic is found to contain the highest harmonic power. Therefore, it is reasonable to expect that the biggest benefit should be obtained by tuning the third harmonic. The Smith Chart of Fig. 6 shows contours of constant PAE when varying the third harmonic load condition. (All other harmonics are still kept to 50Ω.) The optimum third harmonic load is here close to a short and increases PAE from 56 to 61% and $P_{out}$ from 31.5 to 31.8dBm compared to the 50Ω case. To check the assumption that the third harmonic has here the bigger influence, the second harmonic was tuned for optimum conditions, when the third up to the fifth harmonic were set to 50Ω. In this case only a small improvement of 1% in PAE was obtained. As a consequence, those investigations provide new insights in the influence of harmonic load terminations. There is a simple way to determine which of the harmonics should be tuned and if the effort of tuning more than one harmonic is justified. For those decisions only the spectral harmonic content for the device when operated under the large signal conditions of interest (optimised fundamental load, all harmonic loads at 50Ω) has to be known.

## CIRCUIT DESIGN AND MMIC RESULTS

Targeted output power for the GSM MMIC in 50Ω environement was 34dBm at 3.2V and an input power of 3dBm. Additional design targets were an isolation of at least 70dB at $P_{in}$=3dBm when the MMIC is set to its off-state, an analog power control of at least 50dB by varying the base potential, and packaging in TSSOP-10 with heatsink. The design techniques employs two steps. In a first step of the design cycle on-wafer loadpull measurements provide reasonable conditions for output power, which are combined with appropriate small-signal simulations to fix the circuit topology in principal and ensure adequate small-signal characteristics. From the very beginning the package parasitics were included in the design. The size of emitter area required for the output stage was determined from on-wafer loadpull data of 0.5W HBTs which were available at the date of design. The GSM application uses constant envelope modulation so that the amplifier can be driven into hard saturation where highest PAE is obtained. Therefore, from the above specifications a required linear gain of at least 35dB can be estimated. The gain as well as the isolation targets require realisation of a three stage amplifier as shown in Fig. 7. The emitter areas for the transistors in the first, second and third stages were scaled with a factor 1 : 7 : 49. From gain considerations higher factors could be chosen but then due to device tolerances and design inaccuracies the risk increases that one of the driver stages goes into saturation

before the final stage. From the loadpull data the load impedances required for the various stages were estimated and adequate interstage networks designed. The DC blocking capacitors, as well as the bond and lead inductances of the various collector biasing networks were implemented in the interstage network design. Circuit stability was ensured by using small resistors at the base and RC-feedback networks between collector and base in the first two stages. All those network designs were done by using the HBT model only for small signal simulations until the required small signal performance had been obtained. In a second step of the design cycle further optimisations of the power performance were achieved by large-signal simulations.
The power performance of the MMIC was investigated using an evaluation board where the external fundamental load matching circuit (Z2, C4) was adjusted for optimum performance. The second harmonic was shorted (C3) to fulfill the respective harmonic suppression requirement of <-40dB at the RF-output. For keeping the output matching circuit simple, no third harmonic tuning was used. Fig. 8 shows output power and PAE of the amplifier obtained at the connectors of the evaluation board as a function of the power control voltage. An output power of 2.7W is achieved with a single supply voltage of 3.2V. The maximum large signal gain is in excess of 32dB and the dynamic range for power control exceeds 80dB. Note that this excellent performance is achieved in a tiny plastic package (TSSOP10) which occupies less than one half of the board area compared to packaged GSM devices before.

## CONCLUSIONS

A small chip size InGaP/GaAs HBT MMIC power amplifier housed in TSSOP10 has been developed for low-voltage wireless applications. On an evaluation board the GSM MMIC achieved 2.7W and 56% PAE at 3dBm input power and a single supply voltage of only 3.2V. For the design on-wafer measurements of large-emitter area power HBTs as well as an accurate electrothermal HBT large-signal model have been successfully used. In addition, the on-wafer loadpull measurements provided new insights concerning the influence of harmonic load terminations. A simple method was discussed to decide which of the harmonics should be tuned, and whether the effort of tuning more than one harmonic is justified.

## ACKNOWLEDGMENT

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## TABLES AND FIGURES

| | |
|---|---|
| Emitter Width w | 3 µm |
| Frequencies ft / fmax | 30 GHz / 60 GHz |
| On-Resistance Ron | < 450 Ù/µm² |
| Offset Voltage Uoffs | < 0.2 V |
| Current Gain â | >80 |
| Max. Coll. Curr. Density jcmax | 0.2 mA/µm² |
| Coll.-Emit. Breakd. Volt. Uceo | > 15 V |
| Outp. Pow./Emit.-Area Pout/Ae | 0.3 mW/µm² |

Tab. 1: Device characteristics of HBT 30-process for mobile communications at 3 V.

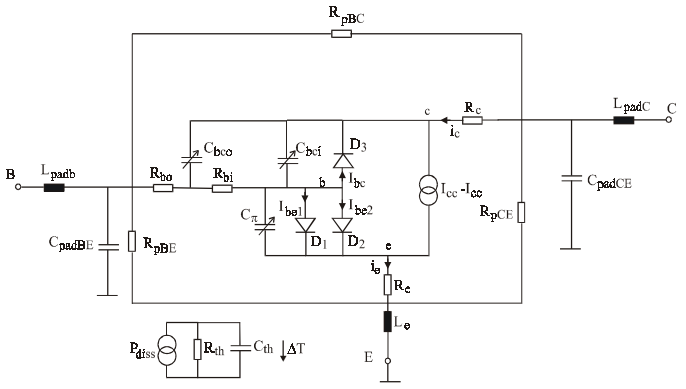


Fig. 1: Electro-thermal large signal model of HBT

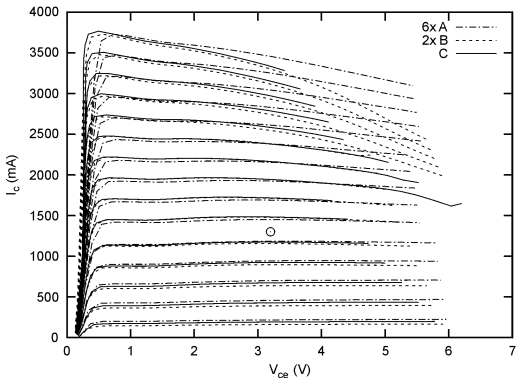


Fig. 2: Scaling of on-wafer measured pulsed (T=0.58ms) IV-output characteristics of large emitter area HBT power stages (A=1440µm², B=4320µm², C=8640µm², o max. operation current)

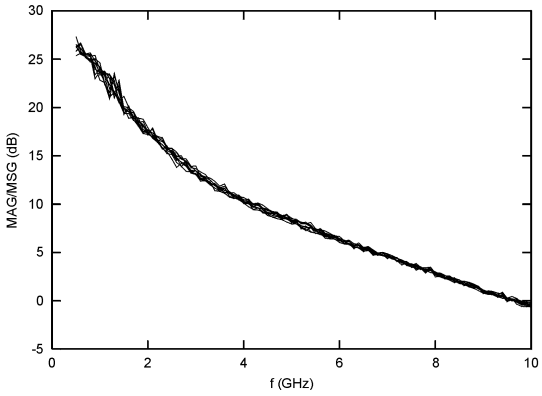


Fig. 3: Maximum available gain for HBTs with 4320µm² emitter area ($V_{CE}$=3.2V, $I_C$=432mA)

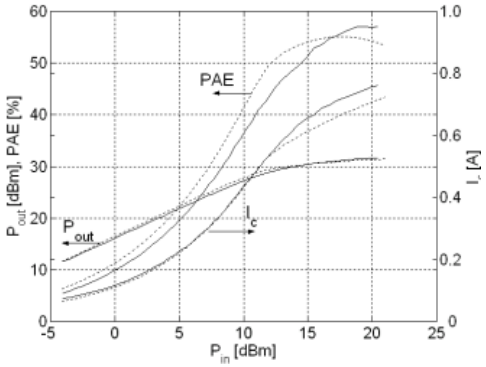


Fig. 4: On-wafer measured power sweep of output power, PAE and $I_C$ of large emitter area power HBT ($A_e$=4320µm², $I_Q$=43mA, $V_{CE}$=3.1V, f=900MHz, harmonic loads=50Ω, simulation: dotted lines)

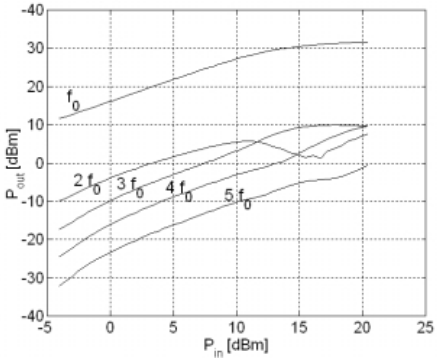


Fig. 5: On-wafer measured power sweep of harmonic output powers of large emitter area power HBT (same conditions as in Fig. 4)

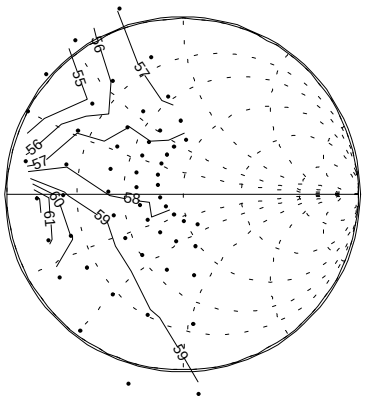

Fig. 6: PAE contours as result from on-wafer loadpull measurements (same conditions as in Figs.4&5, but third harmonic tuned)

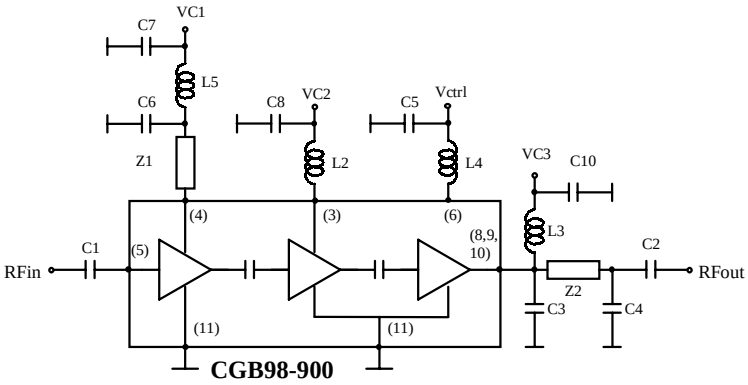


Fig. 7: Circuit schematics and bonding diagram for three stage GSM HBT power MMIC as well as external circuitry on evaluation board

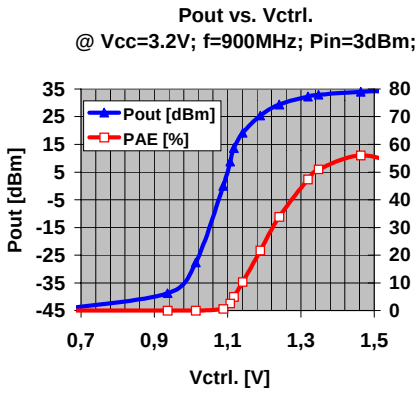


Fig. 8: Output power $P_{out}$ and power added efficiency PAE as a function of power control voltage for GSM HBT power MMIC