TRANSIT TIME MESFET PHASE SHIFTER

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ABSTRACT

The phase shift of a signal through a common-source MESFET can be changed with little effect on the amplitude by altering the gate-drain spacing. The feasibility of employing this principle to realize a highly compact,monolithic phase shifter has been investigated. The behaviour of the devices with differing gate-drain spacing has been measured and modelled and a design for a monolithic implementation is presented.

Keywords: Phase shifter, MESFET, application

1.INTRODUCTION

The principal causes of signal delay in a MESFET are the propagation delay through the length of the gate and the charging time of the depletion region. Through an understanding of the changes in the depletion region as a function of the geometry (Ref.1), changes in phase shift through the device can be predicted. With a constant drain current I_d, these changes will have a major effect on the gate-drain capacitance C_{gd}, gate-source capacitance C_{gs}, and transconductance delay τ, as well as affecting g_{ds} and R_d.

In order to investigate the feasibility of using these effects to realize a phase shifter, a study has been conducted using a standard, commercially available, GaAs MESFET with gate-drain spacing increased from the normal value by 0.5 and 1.0 μm.

A physically-based small-signal equivalent model has been extracted from scattering parameters for the three devices and the values of the first-order model elements checked by comparison with a quasi-2D physical simulation (Ref.2). A transit-time phase shifter is realized by connecting two matched MESFETs with different gate-drain spacing in parallel and changing the phase shift by turning on one of the two devices.

2.MODEL

A small-signal equivalent circuit model with the elements based on physical parameters is used. As a first approximation the dependence of the element values on small changes in gate-drain distances is considered. The physical equations used to approximate the change in the space-charge depletion layer extension, at a fixed bias point in the saturation region, as a function of small incremental increases in the gate-drain distance, (Ref.1).

$$C_{gd} \approx \frac{2\epsilon Z_g}{1+\frac{2X}{L_g}} \qquad (1)$$

$$C_{gs} \approx \frac{\epsilon Z_g L_g}{d}\left(1+\frac{X}{2L_g}-\frac{2d}{L_g+2X}\right) \qquad (2)$$

$$\tau \approx \frac{1}{\upsilon_{sat}} \left(\frac{X}{2} - \frac{2d}{1 + \frac{L_g}{2X}} \right) \tag{3}$$

$$R_d \approx \frac{L_{gd} - X}{qN\mu_o W Z_g} \tag{4}$$

$$g_m \approx f(\upsilon_{sat}, Z_g, d) \tag{5}$$

$$R_i \approx f(\upsilon_{sat}, L_g, I_{CH}) \tag{6}$$

$$R_{ds} \approx f(R_{sc}, L_{gd}, X) \tag{7}$$

$$C_{ds} \approx f(C_{sc}, L_{gd}, X) \tag{8}$$

Where the essential dimensional parameters are defined as shown Figure 1:

Z_g is the gate width
L_g is the gate length
L_{gd} is the gate-drain separation distance
X is the extension of the gate-drain depletion layer into the gate-drain space past the gate edge
W is the thickness of the N-layer
d is the thickness of the depletion depth

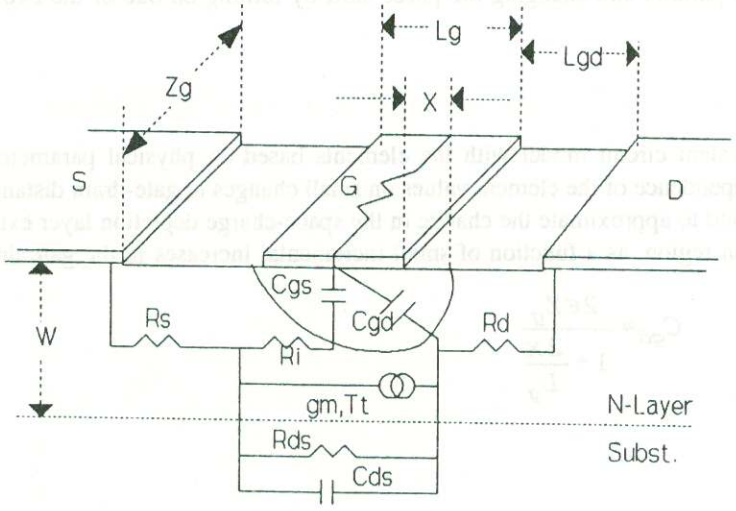

Figure 1: *Dimensional parameters for the small-signal model*

General simplifying assumptions include: uniform channel doping, fixed surface potential energy, abrupt depletion region boundaries, and fixed g_m and R_i. Note that Eq.5 is strictly not correct since there is a dependence of g_m on V_{ds}. However, assuming g_m is a function only of channel doping and gate bias only, leads to a good first order approximation. For similar simplifying reasons it was assumed that R_i is fixed, for small incremental increases in the gate-drain distance, hence, as shown in Eq.6 R_i is not a function of L_{gd} or X. Note that R_d in Eq.4, the drain resistance in the bulk drain region, is the only extrinsic element to vary with X. Geometric capacitive coupling between the gate and drain is less than 10% (Ref.3). For the small incremental changes in gate-drain distances in the order of 1.0 μm this was neglected.

Both R_{ds} and C_{ds} are difficult to define or calculate from physical data. Uncertainties in the surface potential energy cause uncertainties in the depletion-layer size and shape, which in turn relates to uncertainties in the electric fields within the device, and finally the calculation of R_{ds} and C_{ds}. The approximations, are based on a one-dimensional change in the depletion layer extension into the gate-drain space. These approximations break down when calculating R_{ds} and C_{ds}. Changes in depletion layer thickness should also be considered but would result in a loss of simplification. In order to maintain the simplicity of the approximation, R_{ds} and C_{ds} were approximated by an empirical linear constant scaled by X and optimized to fit the measured data (Ref.4). Both R_{sc} and C_{sc} in Eq.7 and Eq.8 refer to the substrate resistance and capacitance respectively for a standard device with no change in the gate-drain distance.

3.DISCRETE MODELLING RESULTS

Table 1 is a summary of measured and physical modelled data. The measured data is presented as an empirically matched small signal model. The "Ref" column refers to a standard commercially available 0.5 μm ion-implanted depletion mode MESFET made of 6 gate fingers each 50 μm wide. The "+0.5" and "+1.0" columns are devices with an increase in the gate-drain distance of 0.5 μm and 1.0 μm respectively.

Plots of empirical versus physical S_{21} data are shown in Figure 2 and Figure 3. Shown is the change in magnitude and phase for different gate-drain spacings normalized to a standard foundry library MESFET,column 1 of Table 1.

	Empirical data			Physical model			units
G-D Spacing	Ref	+0.5	+1.0	Ref	+0.5	+1.0	μm
C_{gs}	360	410	470	340	420	480	fF
C_{gd}	40	29	21	42	28	22	fF
C_{ds}	80	80	80	80	80	80	fF
R_{ds}	430	550	700	400	500	600	ohm
R_i	4.4	4.6	4.8	4.5	4.5	4.5	ohm
g_m	37.5	36.9	36.3	37	37	37	mS
τ	3.5	4.4	5.5	3.1	4.3	5.2	ps
L_g	35	37	39	35	35	35	pH
R_g	1.0	1.0	1.0	1.0	1.0	1.0	ohm
L_d	21	15	11	18	18	18	pH
R_d	1.2	0	0	1.9	1.4	1.1	ohm
L_s	3.5	4.7	6.3	4.0	4.0	4.0	pH
R_s	1.2	1.4	1.6	1.3	1.3	1.3	ohm

Table 1: *Empirical and physical modelled small signal equivalent circuits*

Phase is particularly well modelled with most inaccuracies occurring in the magnitude of S_{21}. Similar results exist for the other S-parameters. The discrepancies between the measured and modelled results are thought to be primarily due to the simplifying assumptions made in development of the analytical expressions.

4.MMIC PHASE SHIFTER DESIGN

4.1 Realization

The design is based on a commercially available, 0.5 μm ion-implanted depletion mode MESFET process and a phase shifter was realized by connecting two matched MESFETs in parallel, Figure 4. Both MESFETs are identical in all respects except for a 1.0 μm increase in the gate-drain spacing of one of the devices. The input signal is fed to the gates of both MESFETs in parallel. Gate and drain voltages are turned on to power the desired MESFET resulting in a phase shift.

Although not employed in the present design, it should be possible to achieve an overall gain through the phase shifter. Several devices will have to be cascaded to realize any required value of phase shift; this design study suggests that a complete 4-bit phase shifter with a range up to 360 degrees at 20 GHz could be realized in an area as small as 1 mm^2.

A potential problem with this type of design is the sensitivity to gate-drain alignment. Properly aligned MESFETs in a well-controlled process are typically within 0.2 μm of the desired spacing. The results from the model indicate that a 0.2 μm tolerance will result in a phase uncertainty in the absolute phase of 4 degrees at 20 GHz.

4.2 Results

The MMIC version, as fabricated (shown in Figure 4), was found to have a large gate-drain misalignment resulting in a shift of the drain contact with respect to the gate fingers. Since the layout employs two gate fingers on either side of each drain contact, the increase of gate-drain spacing on one side is cancelled by a decrease on the other side. Thus, although there was a phase shift of about 10 degrees in the band from 15 to 20 GHz, the performance of the chip was not correctly predicted by the model.

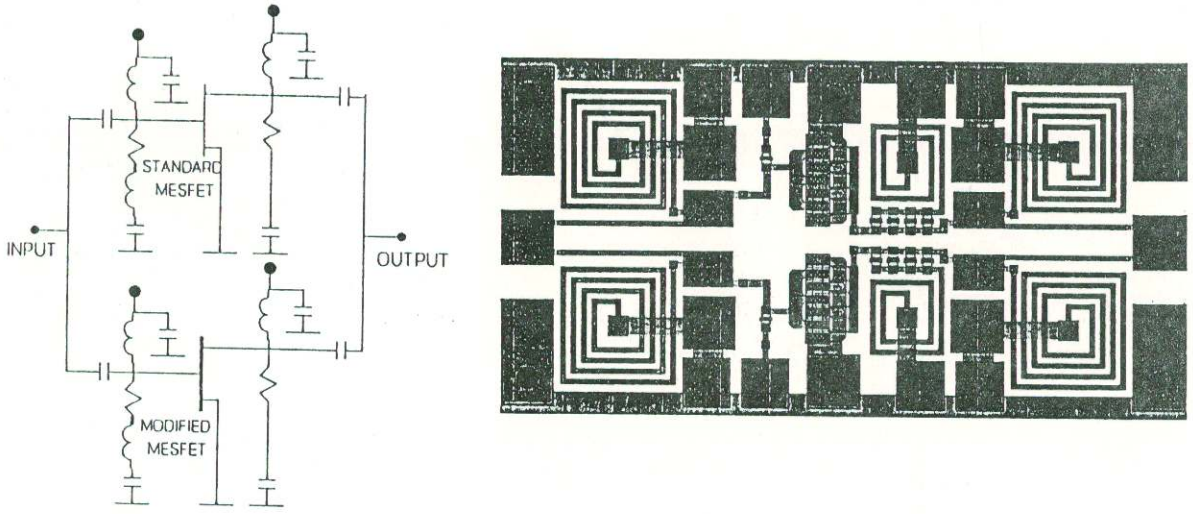

Figure 4: *Schematic and layout of the MMIC transit time phase shifter concept.*

5.CONCLUSIONS

Modifications to the gate-drain spacing of a standard MESFET have been shown theoretically and experimentally to change the phase shift through the device. With an increase in the range 0.5 to 1.0 μm, a phase shift of 10 degrees can be realized at 20 GHz. A monolithic implementation has been produced which demonstrates the feasibility of the transit time phase shifter concept, although the prototype did not perform as predicted by the model owing mainly a gate-drain alignment problem. The concept does not use delay lines and therefore offers the possibility for the fabrication of highly compact monolithic phase shifters.

6.ACKNOWLEDGEMENT

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7.REFERENCES

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