HIGH RESOLUTION PHASE SHIFTER FOR ACTIVE PHASED ARRAY ANTENNA BEAM FORMING

Heinz-Peter Feldle, Rolf H. Reber
Telefunken Systemtechnik, Airborne Systems Division
Sedanstr. 10, 7900 Ulm, Germany
Phone Int.-0731-392-3219, Telefax Int.-0731-392-3073

ABSTRACT

The paper describes the design and measurement results of a monolithic single chip phase shifter. This broadband, 6-bit phase shifter exhibits very low overall insertion loss with remarkably low variation, good VSWR and exceptional phase performance with only 2.4 degrees RMS phase error over all 64 phase states across the entire 5 - 6 GHz band. Moreover the digital design leads to good stability with regard to temperature and voltage variation. These excellent performance data lead to minimum driver levels and high efficiency in Tx-mode, a distinct reduction of the noise figure in Rx-mode for the complete T/R-module and allow minimum calibration effort of the active phased array.

Keywords: MMIC Phase Shifter, T/R-Module, Active Phased Array

1. INTRODUCTION

Modern multifunctional active phased array antennas for ground, ship and space based applications consist of thousands of radiating elements. Each of them is driven by a solid-state Transmit-Receive (T/R) module (Fig. 1). One of the essential control components in a T/R module is the phase shifter. This key device provides the phase control needed for pattern generation, beam steering and polarization setting. Particular requirements on such a phase shifter are high phase resolution, low insertion loss with minimum variation and low input/output return loss. Especially for airborne applications with densely integrated T/R-modules such a device should be small and consume a negligible amount of power.

2. CIRCUIT DESIGN AND MANUFACTURING

Starting with an extensive analysis of discrete and integrated phase shifter concepts, the best solution for the demands stated above turned out to be a switched filter configuration [1, 2, 3, 4]. In the 180 degree bit two SPDT-Fet switches select a T-type high pass or low pass network in the signal path. The circuits for the 90, 45 an 22.5 degree bits use bridged-T networks where the switching FETs become part of the phase shifting filter. For the two bits with the lowest phase shifts the circuit consists of a switched capacitor or an inductor, which form together with the line impedance the required high pass or low pass filter. The FETs are controlled by a voltage of 0V and - 5 V respectively, where every bit needs two complementary signals.

Compared to other phase shifter designs the low value of control voltage simplifies the design of ASICs for T/R-module controlling, because most ASIC manufacturers can not provide circuits with output voltages lower than - 5 V.

Integrated gate resistors provide isolation between the RF and the control logic. In order to allow simple generation of the control voltages and to prevent static charging of the transistor gates, pull down resistors to ground were supplied at every control pad.

A commercial CAD-program was used to simulate and optimize the individual bits and the complete circuit of the phase shifter (Figure 2). Also the chip layout has been generated by using this software. The RF-ports were completed with adjacent via holes to enable on-wafer probing with coplanar tips. All control pads are aligned at one side of the chip to simplify control board layout and a later integration of driver-converter circuits.

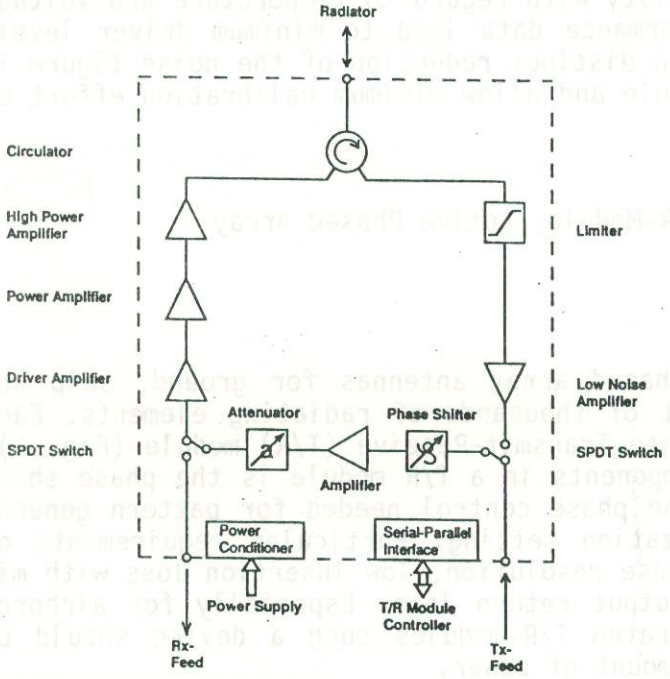

Fig. 1 T/R-Module Architecture

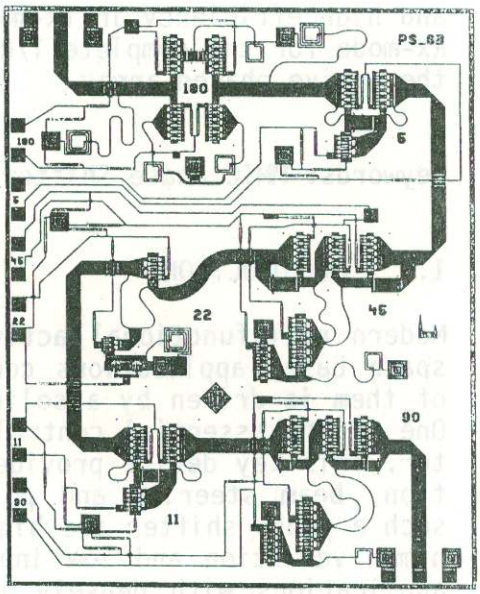

Fig. 2 Photograph of the 6-Bit Phase Shifter

The phase shifter was processed at the in-house foundry using their standard "E05V" process. This process employs 0.5 µm recessed gate MESFET technology and uses MOCVD grown expitaxial layers for the FETs and resistors. A silicon nitride layer is used for passivation and forms the dielectric of the capacitors.

3. PERFORMANCE

The realized 6-bit phase shifter chip shown in Figure 2 occupies a chip area of 3.8 mm x 3.0 mm. The circuit consists of 21 MESFETs with 0.5 µm gate length and a total gate width of 16 mm. Several chips have been measu-

red in a dedicated test fixture to allow TRL calibrated measurements. Additionally some chips have been tested by wafer-probing. An in-house test equipment controls the phase shifting bits and records the S-parameters.

The measured performance at all 64 phases states over the entire 5 - 6 GHz band is shown in Figure 3. For the reference state all bits are switched to the low pass state.

Table 1 summarizes the essential data of this phase shifter chip.

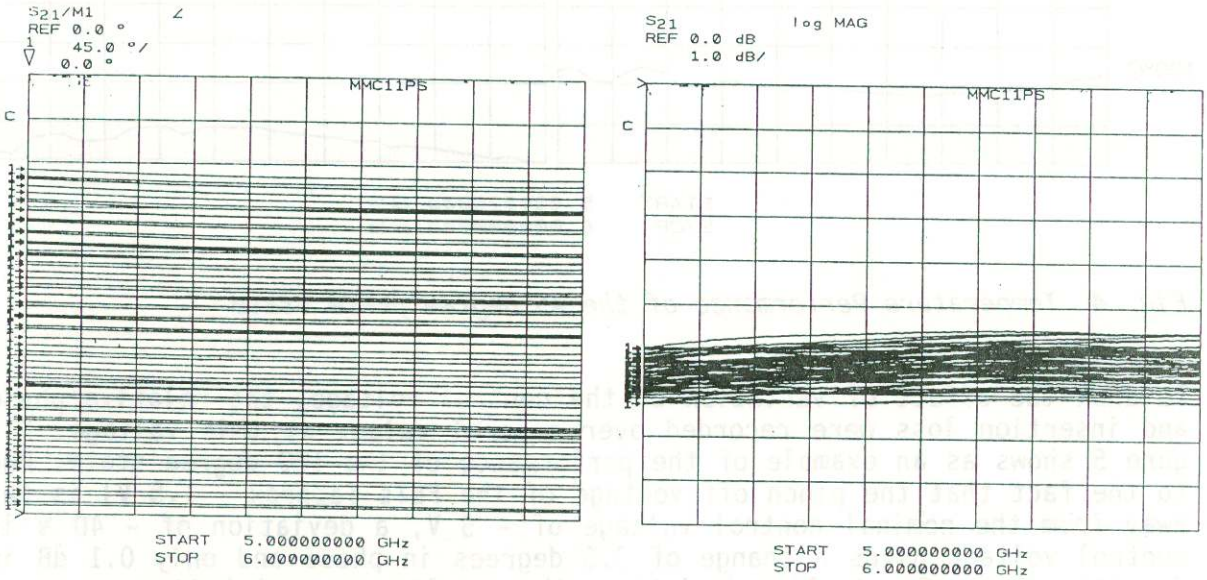

Fig. 3 Measured Performance (all States)
a) Relative Phase *b) Insertion loss*

Frequency	5 - 6 GHz
Phase Shift	6 Bit
Insertion Loss	6.4 dB
Insertion Loss Variation	± 0.9 dB
RMS Phase Error (all states)	2.4 Deg.
Input/Output Return Loss	≤ - 11 dB
DC Control Voltage	0 V and -5V (complementary)
Chip Size	3.8 mm x 3.0 mm x 0.15 mm

Table 1: Phase Shifter Performance (25° C)

To evaluate the performance over temperature, chips were bonded in housings. Figure 4 shows as a typical result the measured relative phase and insertion loss for 23° C, 50° C and 100° C at the 45° state. The change in phase over temperature is about 0.09 deg/° C, the insertion loss increases with 0.015 dB/° C. The phase reference in Figure 4 is the low pass state for all bits measured at 23° C.

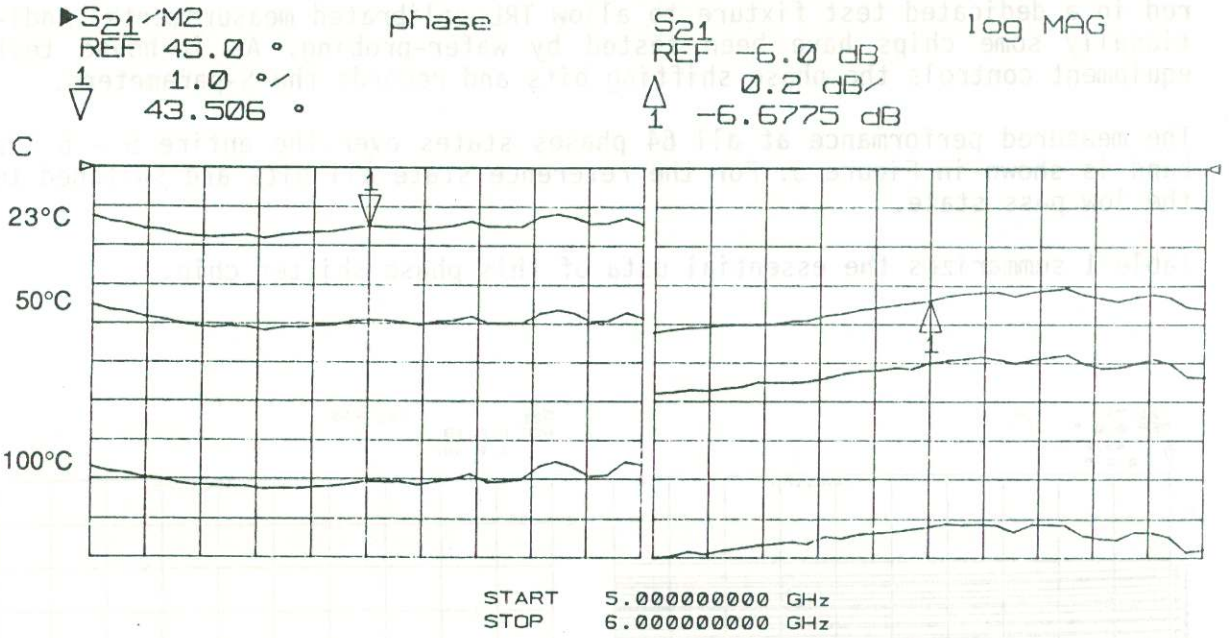

Fig. 4 Temperature Performance of the 45 degree phase state

To show the effect of variation of the control voltage, the relative phase and insertion loss were recorded over several values at this voltage. Figure 5 shows as an example of the performance of the 180 degree state. Due to the fact that the pinch off voltage of the FETs (approx - 1.5 V) is far away from the nominal control voltage of - 5 V, a deviation of - 40 % in control voltage gives a change of 3.5 degrees in phase and only 0.1 dB in insertion loss. For smaller deviations the results are much better.

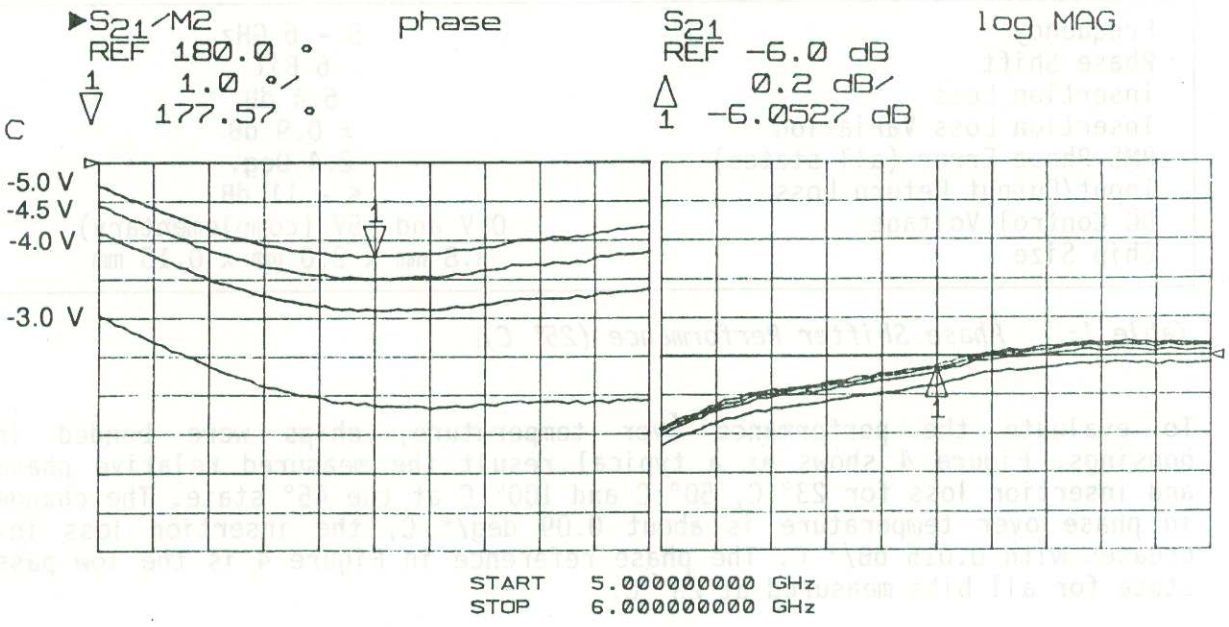

Fig. 5 Deviation of relative phase and insertion loss vs. control voltage

Several chips have been tested with a wafer-probe station, to get information about the uniformity over different wafers. In Figure 6 the relative phase and the insertion loss from the 11.25, 22.5 and 45 degree state of the phase shifter were plotted. A maximum phase deviation of ± 1.5 degrees or better can be seen for the 11.25 and 45 degree state; the 22.5 degree state is less sensitive to wafer tolerances.

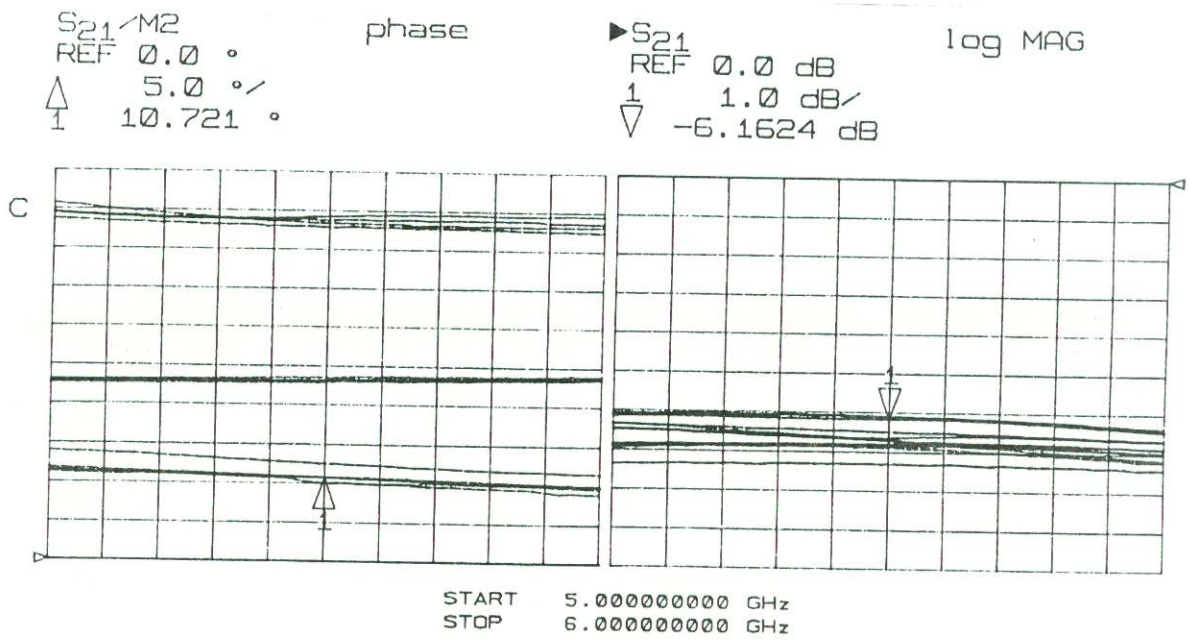

Fig. 6 Uniformity of 11.25, 22.5 and 45 degree state on different wafers
a) relative phase *b) insertion loss*

4. CONCLUSION

The design, fabrication and sucessful RF measurement results of a monolithic C-Band 6-bit phase shifter have been described. This chip shows very low insertion loss, good VSWR and exceptional phase performance in addition with low insertion loss variation. Furthermore the phase and amplitude variations with temperature and control voltage are very small due to the digital structure of the phase shifter. These excellent properties, together with small size, fast switching time and negligible power dissipation make this chip a good choice for an active phased array for ground, ship and space applications.

5. REFERENCES

1. R.B. Carver, "Broadband Diode Phase Shifter", *IEEE Trans. Microwave Theory Techn.*, Vol MTT-20, pp. 314 - 323, May 1971

2. B.X. Varman, "New circuit configurations for designing 0 - 180° digital phase shifters, *IEE Proceedings*, Vol. 134, No. 3, June 1987

3. K. Wilson et. al., "A Novel MMIC-X-Band Phase Shifter", *IEEE Trans. On Electron Devices*, Vol. ED-32, pp. 2741 - 2747, Dec. 1985

4. J.R. Selin, "Continuously Variable L-Band Monolithic GaAs Phase Shifter", *Microwave Journal*, pp. 211 - 218, Sept. 1987