AN OVERVIEW OF GaAs MMICs RELIABILITY

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ABSTRACT

This work intends to give an overview of the most important reliability issues for GaAs MMICs; in particular, aspects such as reliability procedures and predominant failure mechanisms will be discussed, highlighting the differences with those of discrete FETs; some of the most relevant reliability figures available from the literature will be presented; finally some comments will be given on common reliability programs running in U.S. and Europe for these devices.

Keywords: MMIC, reliability procedure, accelerated testing, failure mechanims.

1. INTRODUCTION

The possible application areas for GaAs MMICs are widespreading, even though higher market penetration was forecast few years ago (see for example [1]): military programs are running in U.S., telecom companies are beginning to extensively use MMICs in radio links equipment and consumer applications such as DBS and mobile telephony seem to open the possibility for high volume production.
Even if GaAs has some advantages over Si concerning performances and power comsuption, other key factors should be carefully addressed in case of large quantities, one of these factors surely being reliability.
In the present work, MMICs reliability aspects are discussed, with the following guidelines: first the problem of reliability procedures will be highlighted in chapter 2, with special emphasis to what is peculiar to MMICs with respect to FETs; then failure mechanims will be presented and some of the most significant reliability figures will be discussed; finally common programs running on reliability in U.S. and Europe will be introduced.
External effects such as ESD and radiation will not be considered, even if they are not negligible and a lot of work have been performed in these fields; in particular, ESD sensitivity have been studied [2-3] indicating that the sensitivity to reverse pulses is high, with threshold voltages in the range of few hundreds volts; this is not unexpected, as FETs are the most sensitive components, and they are known to be sensitive to the same voltage levels, at least [4]. A reliability problem could be the existance of latent failures, that were excluded in [2], while, speaking of FETs, the possibility that "walking wounded" failures may go into system application was pointed out in [4]. Regarding radiation hardness, this is generally considered a GaAs reliability advantage over Si, and functional insensitivity up to 120 MRad total dose have been reported [5].

2. RELIABILITY PROCEDURES

Sometimes, MMICs reliability is directly associated with the one of FETs (and

indeed a lot of works tend to demonstrate that FETs limit MMICs lifetime), nevertheless some features are specific of ICs and are not addressed during FETs accelerated testing; in particular we refer to:

- presence of passive components
- possible proximity effects (interactions between adjacent elements)
- impossibility to have direct access to each element (circuit complexity)

These items have to be kept in mind when designing reliability procedures and they will be the core of our next discussions.

2.1 IC element testing

A well known way to start MMIC reliability investigation is to assess reliability of each element that appears into the final circuit (see for example [6]); this means to perform thermal and electrical accelerated tests on resistors, capacitors, metal layers, interconnections and airbridge, diodes and FETs; the purpose is twofold: from one side the results are useful as indicators for process quality and related possible improvements, from the other side it would be highly desiderable to correlate MMICs lifetime to the extrapolation coming from the evaluation of each element.
To a certain extent, this is possible [6] even if it is probably limited to the case when an element is present on the MMIC with stress conditions much higher that the others; analysing elements reliability, a lot of failure mechanisms are involved (metal-GaAs interaction, surface degradation, traps related effects, electromigration, dielectric breakdown, mechanical degradations) each having its own dependance on accelerating stress; the correlation with real operating conditions of MMICs is surely difficult. As on example, Tab. I reports accelerating factors for various elements.
A particular case is the investigation on proximity effects, that requires the availability of a basic FET plus one (or more) sidegate contact [7]; it is important (and it is valid for all elements testing) that the structure is designed and realized at the limits of design rules: to that purpose it is becoming common for foundry users to design specific test circuits called TCVs (Technological Characterization Vehicles) that can give more specific informations than those coming from standard foundry PCMs [8].

TYPE	n	Ea (eV)	V
Metals	1.5	2.24	-
Air Bridges	4.5	0.43	-
Resistors	1.3	1.0	-
Ohmics	3.5	?	-
FETs	-	2.6	-
CAPs	-	?	>2

Tab.I : example of accelerating factors for elements, expressed by means of current exponent (n), voltage exponent (V) and activation energy (Ea) [6].

2.2 MMIC testing

Accelerated testing of complete circuits poses specific problems not commonly addressed during discrete FETs testing.
One controversial point is the suitability of DC or RF lifetesting: especially in U.S., there is a growing interest for RF lifetesting which is reported to give "worst case" predictions closely correlated with actual operating conditions [9]; from the other side DC lifetesting is more simple and reproducible and it is largely used too (as shown in the next chapter).
Up to our knowledge, there is no available result coming from DC and RF lifetesting of the same circuit under comparable conditions, in other words, it is not easy to demonstrate that RF operation induces specific failure mechanisms; as a general statement, aspects such as electrical functionality should be considered: for example, especially for complex circuits, RF operation can significantly change the aging conditions. Anyway, the overall problem is not clear and recent data show no degradation during RF test performed under 2 dB power compression conditions [10].
A different problem is failure criteria definition: supply current often is the only available DC parameter and the choice of RF criteria is mandatory; moreover, users feel more confortable with them, as they give a direct indication of circuit functionality.
It is curious to see that sometimes RF based criteria are reported to be more severe than DC ones [9], while in other cases rapid DC parametric degradation seem to have little influence on dynamic performances [11]; again, it is probably difficult to give general rules, as circuit electrical design has to be considered. With the aim to avoid these problems, there are suggestions to use specific test circuits, called DECs (Dynamic Evaluation Circuits) which allow for dynamic characterization, maintaining the technological critical points of the final MMICs without great circuit complexity [12]; this approach looks very similar to the one being followed for Digital IC reliability program in U.S. [13].
An original work concerning both lifetesting and failure criteria is given in [14]: DC biased thermal step stress is used for complete MMICs both increasing and decreasing temperature; the main conclusion is that DC and RF failure criteria are coherent and indicate the presence of a single failure mechanism, and the overall results are reported to be in agreement with those from RF lifetesting.
A third critical point is the determination of actual chip temperature [15]: without entering into the details of the 3 methods widely used for FETs (ΔVgs, Infrared Thermography and Liquid Crystals) it is clear that the electrical method is generally not suitable for MMICs, so that the combined use of the other two methods is recommended; it seems reasonable to consider also overheating problems due to RF operations.
While people generally think that FETs are mainly responsible for overheating, reliability problems due to temperature increase on NiCr resistors were reported [6]; in this case thermal mapping can be considered a tool for design optimization.
As a general comment to this chapter, it is worth saying that initiatives exist in U.S. and Europe, with the aim to give standardized approach for MMICs reliability evaluation [12,16].

3. MMIC FAILURE MECHANISMS

It is easy to say (as it will be shown in the paragraph 5) that most of the failure mechanisms responsible for MMICs degradation are related to FETs; gate

semiconductor interaction is probably the most common mechanism, but reports exist on ohmic contacts degradation [17], surface related problems [7,9,18] and hydrogen effects [19]; as extensive discussions on these mechanisms are already available (see for example [20]) we will concentrate on what is specific to MMICs.

3.1 Proximity effects

Even if a huge amount of work exists on ICs functional drawbacks due to sidegating (or backgating), it is not clear whether these phenomena have reliability implications, i.e. very few informations are available about their degradation with temperature.
A preliminary work [21] reported short term degradation of backgating threshold voltage during storage at high temperature 290-350°C), but very recently [22] sidegating insensitivity during long term unbiased (250°C) and biased (230, 250°C) tests has been demonstrated; our own experience is similar to the former one, with backgating degradation measured during thermal step stress, at temperatures higher than 300°C (Fig.1).
Maybe the available results are not controversial if we consider that degradation could be limited to very high temperature, but a definitive conclusion requires further work.

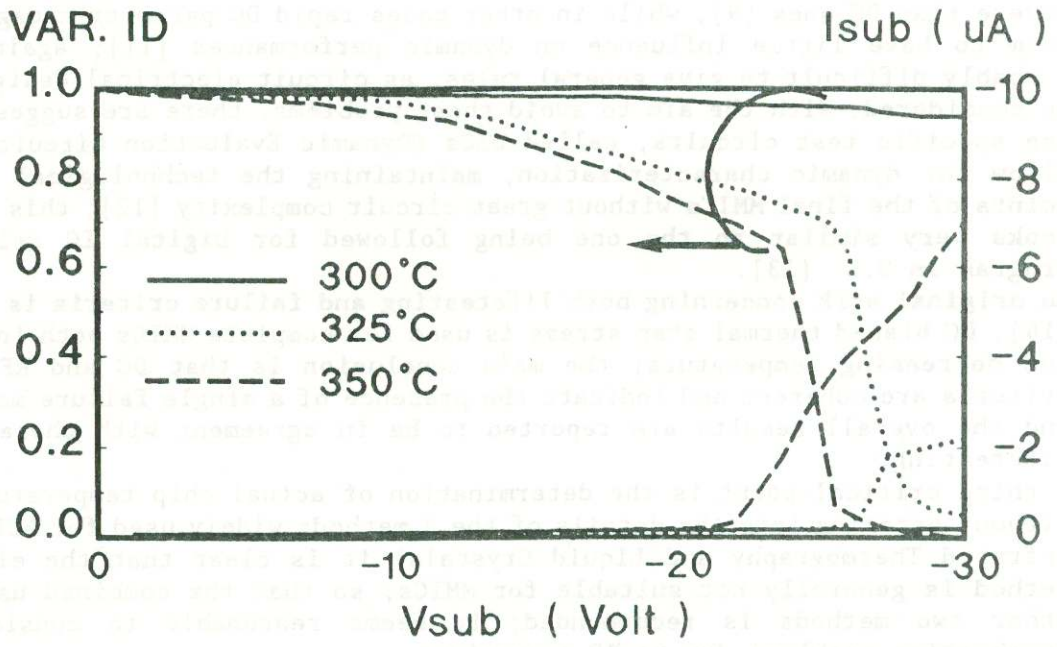

Fig.1 Degradation of backgating characteristics during thermal step stress (the behaviour of drain and substrate current is reported).

3.2 Passive components degradation

It is generally believed, and it is demonstrated by element testing, that passive components reliability is much higher then the one of active devices; however, this cannot be considered a general statement, because circuit layout

and bias conditions can significantly affect the reliability of passive components.
In [6] it was reported that lifetime of a MMIC amplifier was dominated by a NiCr resistor, which was 65°C hotter than the FETs.
Degradation of off-chip capacitors and on-chip TaN resitors (due to Ga autodiffusion) was responsible for early failure distribution of MMICs, with mean lifetime 2-3 times less than the one of main population, determined by ohmic contact degradation [17].
Metal bridging between ohmic contacts and first level interconnecting lines were found during MMICs lifetest [23], attributed to decrease of S.I. GaAs surface resistance; in this case, the failures were confirmed during element testing and an activation energy of ≈ 1 eV was calculated.
MIM capacitor failures were mentioned too [24] even if they could probably be related to process defects, such as SiN pinholes.

4. RELIABILITY FIGURES

Tab. II summarizes some of MMIC reliability results: it does not want to be a complete overview of what is available, but we would only like to give an understanding of the most significant and complete results.

Ref	Device	Test	Fail. Mechanism	MTTF (at T°C) (hrs)	Act.Energy (eV)
[25]	ASIC and MMIC	DC	Gate sinking	$2.5*10^6$ at Tch=150°C	1.6
[26]	Trans.Imp.Ampl.	DC	-	$8*10^6$ at Ta=75°C	1.1
[27]	S-band MMIC	Storage and RF	Surface effects	$0.35*10^8$ at Tch=130°C (1)	1.4
[28]	Ku-band MMIC	DC and RF	Gate sinking	$2.1*10^8$ at Ta=75°C	1.65 (1)
[23]	1GHz Prescaler	DC	Interconn. bridging	Fail.rate <25 FIT at Tch=120°C	1.1
[11]	IF Amplifier	DC	Gate sinking	10^7 at Ta=120°C	1.9
[29]	2-6 GHz Ampl.	DC	Gate sinking	$3.2*10^6$ at Tch=120°C	1.2
[9]	X-band Ampl.	RF	Surface effects Ohmic degrad.	$2*10^4$ at Tch=125°C	0.5
[17]	2-8GHz Ampl.	RF	Ohmics and passives degrad.	$2.3*10^3$ at Tch=175°C (2)	-

Note 1 : Extimation from element testing
2 : Bimodal distribution

TAB.II Summary of available reliability figures.

Most of the data involve only FET degradation, with energy associated high activation energies, which are known to give over-optimistic extrapolations; in [9] a low activation energy was found; one way to exclude the presence of low activation energy mechanisms is to perform long-term, low temperature tests that are available in [11].
There is no clear understanding regarding complexity, that does not seem a reliability issue [6].

5. CONCLUSIONS

Even though reliability figures for MMICs are generally quite good, as they are considered most of the time to be similar to those of FETs, several reliability issues are still open, as discussed in the previous paragraphs. Nevertheless it is very important to see efforts towards standardization both in U.S. and Europe [12,16] under the partnership of JEDEC and ESA, and it has to be underlined that common programs are running concerning MMICs reliability: in particular, under the MIMIC program funded by DARPA, activities are going on towards a complete reliability assessment of the final circuits, including materials and processes assessment, modules evaluation, ESD effects and radiation hardness. In Europe we should mention the work driven by ESA for the definition of capability approval rules [30], and the activities that are going on under ESPRIT 5018 and 6050 projects, for reliability evaluation of low noise and power MMICs manufactured by european foundries.

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REFERENCES

[1] S.Gourrier "Analog Microwave monolithic III-V ICs: Industrial and technical aspects" in Proc. of GaAs IC Symp. 90, New Orleans, Oct.90.

[2] A.L.Rubalcava "Electrostatic discharge effects on Gallium Arsenide ICs", Proceedings of EOS/ESD Symposium 1986, pp 159-165, Las Vegas, Sept. 86.

[3] T.M.Biledeau and C.R.Thomas "The electrostatic discharge sensitivity of GaAs MMIC Amplifiers", Proceeding of EOS/ESD Symposium 1990, pp 131-136, Orlando Sept 90.

[4] A.J.Franklin and V.M.Dwyer "ESD degradation in GaAs MES structures", Solid State Electronics, Vol.34, No 10, pp. 1091-1102, 1991.

[5] M.F.Peters and A.L.Rubalcava "Reliability characterization of a production GaAs MMIC amplifiers - Methodology and results", presented at GaAs Reliability Workshop, Nashville, 1988.

[6] W.J.Roesch and D.Stunkard "Proving GaAs reliability with IC element testing", presented at MAN-TECH Conf., Nashville, Nov. 88.

[7] J.M.Dumas "A survey of the parasitic effects and degradation mechanisms affecting the GaAs FET based ICs", in Proceeding of ESA Electronic Components Conference, pp 93-99, Noordwijk, The Netherlands, Nov. 90.

[8] A. Beusoussan et al "Qualification strategy for multi-chip packaging for space applications", ibidem pp. 145-148.

[9] W.T. Anderson and A. Christou "Status of compound semiconductor device reliability" in Semiconductor Device Reliability, pp. 423-427, A.Christou and B.A. Unger (eds), Kluwer Publ., 1990.

[10] K.Decker "Reliability of Power MMICs Subspected to 2 dB RF Compression", presented at GaAs Reliability Workshop, Monterey, Oct. 91.

[11] R.Esfandiari et al. "Accelerated Aging and Long Term Reliability Study of Ion-Implanted GaAs MMIC IF amplifier", IEEE Trans. on Electron-Devices, Vol.37, No 4, pp. 1174-1177, April 90.

[12] M. Belfort et al., "A methodology for the space qualification of GaAs MMICs" CNET Technical Note, Nov.91.

[13] W.E.Yamada et al "GaAs Digital IC Reliability program", Presented at GaAs Rel. Workshop, Monterey, Oct. 91.

[14] B.Van Rees et al. "MMIC Reliability assesment using step stress testing" presented at ESA/ESTEC Workshop on MMICs for Space Applications, Noordwijk, March 90.

[15] W.J.Roesch "Thermo-Reliability Relationship of GaAs ICs", proceedings of GaAs IC Symposium, Nashville, Nov.88.

[16] B.W. Marks "Proposed JEDEC Guidelines for FET and MMIC Life Tests" presented at GaAs Reliability Workshop, New Orleans, Oct.90.

[17] A.Christou and P.Tang "Failure distribution functions for GaAs MMICs" proceeding of ESREF 91, pp 423-434, Bordeaux, Oct. 91.

[18] K.A. Christianson and W.T.Anderson "Failure analysis of a life tested GaAs MMIC Amplifier" presented at GaAs Reliab. Workshop, Monterey, Oct. 91.

[19] W.O.Camp et al "Hydrogen effects on reliability of GaAs MMICs" in Semiconductor Device Reliability, pp.471-477, A.Christou and B.A. Unger Eds, Kluwer Publ, 1990.

[20] F.Magistrali et al "Failure mechanisms of GaAs MESFETs and Low Noise HEMTs", ibidem pp.261-268.

[21] D.C.D'Avanzo, "Proton isolation for GaAs Integrated Circuits", IEEE Trans. on Electron Devices, Vol. ED-29, No7, pp.1051-1058, July 81.

[22] H.Cholan et al., "Long-term effects of sidegating on GaAs MESFETs" to be presented at IRPS 92, San Diego, April 92.

[23] J.Nagano et al "Reliability evaluation of GaAs MESFETs and ICs" Proceeding of ISTFA 89, pp. 329-334, Los Angeles, Nov. 90.

[24] J.M.Dumas "Parasitic effects and degradation mechanisms of GaAs integrated circuits" proceeding of 4th Int.Conf. "Quality in electronic components", pp.120-127, Bordeaux, 1989.

[25] W.J.Roesch and M.F.Peters, "Depletion mode GaAs IC Reliability" Proceeding of GaAs IC Symposium 87, pp. 27-30, Portland, Oct. 87.

[26] M.Spector and G.A.Dodson, "Reliability evaluation of GaAs IC Pre amplifier HIC", ibidem pp.19-21.

[27] K.Katsukawa et al., "Reliability investigation on S-band GaAs MMIC", Proc. of Microwave and Millimeter Wave Monolithic Circuits Symposium, pp.57-61, Las Vegas, 1987.

[28] Y.Onodera et al. "Reliability evaluation on GaAs MMIC components", Proceeding of ISTFA 89, pp. 335-342, Los Angeles, Nov. 90.

[29] J.Chickanosky et al. "Lifetime and failure mechanisms of a 2-6 GHz MMIC Amplifier", presented at GaAs Reliability Workshop, New Orleans, Oct 90.

[30] R.F.B.Conlon et al., "An evaluation program for the capability approval of GaAs MMICs", ESA Electronic Components Conference, pp.85-91, Noordwijk, The Netherlands, Nov.90.