GaAs SURFACE TREATMENTS AND DEVICE APPLICATIONS

A. Paccagnella (§) and A. Callegari (*)

The effects of H_2 and N_2 in-situ plasma treatments prior to the deposition of Schottky contacts or SiO_2 passivation on GaAs have been studied, showing a large dependance of the electrical properties on the cleaning procedure. For Ti/Pt and Al diodes, degraded rectifying characteristics result after room-temperature H_2 treatments, while diode ideality factors as low as 1.01 were achieved in the temperature range 160-240°C. An increase in the barrier height was also observed with increasing substrate temperature during the plasma treatments, in correlation with H indiffusion in GaAs. Φ^{IV} values of refractory WN_x diodes were enhanced by H_2 treatments, up to 0.78 V after 800°C anneals. Improved C-V characteristics of MOS capacitors were found after H_2 plasma and a thin Si layer deposition, after successive anneals at 600 and 400°C.

1. INTRODUCTION

Important parameters of GaAs MESFETs, such as the barrier height of the gate Schottky diode and the gate-drain breakdown voltage, are controlled by the properties of the metal/GaAs or insulator/GaAs interface [1, 2]. Despite their relevance, the properties of the GaAs surface cannot be easily controlled or modified during the device fabrication process. Various procedures have been successfully carried out with the aim of reducing the surface state density in GaAs, as photowashing [3], or high temperature UHV surface reconstructions after the removal of a protective As cap [4]. Nevertheless, they can be hardly transferred and adapted to microdevice fabrication.

Alternative procedures, compatible with technological processes, have been investigated in this work, based on H_2 and N_2 in-situ plasma treatments prior to the metal or passivating film deposition. GaAs substrates conventionally cleaned with wet chemical etch show a surface with O and C contaminations, grown due to the air exposure before the insertion in the vacuum system. When a H_2 plasma is performed at 200°C, surface oxygen can be completely removed [5]. A successive N_2 plasma can lead to the GaAs surface nitridization, and possibly saturation of surface dangling bonds [5]. After the H_2 plasma, passivation of both acceptors and donors is observed [6], due to the H indiffusion and formation of a neutral complex between each dopant atom and H [7].

Plasma pretreatments of the GaAs surface improve the insulator/semiconductor interface [8, 9]. In this work, we extend the investigation of plasma effects to rectifying metallizations currently used for MESFET gates, i.e. Ti/Pt, Al, and WN_x, and for high quality SiO_2 passivating films.

2. SCHOTTKY DIODES

2.1 Ti/Pt AND Al CONTACTS

GaAs substrates Si doped at $2x10^{17}$ cm^{-3} with conventional alloyed AuGeNi ohmic contact on the backside were dipped in a HCl solution for the removal of the native oxide prior to loading into a vacuum chamber. The sample holder was the cathode of an rf plasma system, where the rf plasma cleanings were performed at a pressure of 0.67 Pa. The GaAs surface was exposed to the H_2

(§) Dipartimento di Elettronica ed Informatica, Universita' di Padova, via Gradenigo 6a, 35131 Padova, Italy;
(*) IBM T.J. Watson Research Center, P.O. box 218, Yorktown Heights, NY 10598.

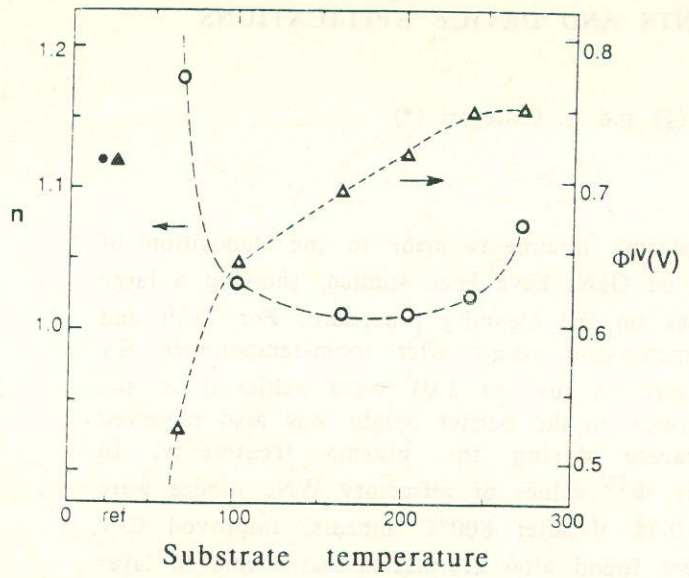

Fig. 1. Ideality factor n and I-V barrier height for Ti/Pt diodes as a function of the substrate temperature during the H_2 plasma.

and N_2 plasma treatments through the circular holes of a metallic mask in contact with the wafer. The same mask was used for the dot definition during the successive Ti/Pt or Al metal deposition by electron-beam, done immediately after the plasma treatments. Substrate temperatures for the plasma treatments and the metal deposition were in the range 24-270°C.

The H_2 plasma effects on the diode characteristics are strongly dependent on the wafer temperature during the treatments. The average values of the diode ideality factor, n, and barrier height, Φ^{IV}, as deduced from the forward I-V characteristics, are reported in Fig.1 as a function of the substrate temperature. As a reference, the average n and Φ^{IV} values for HCl only cleaned samples are reported, too, and do not change upon annealing up to 240°C.

For H_2 plasma treated diodes, room-temperature treatments result in degraded diode characteristics, partially correlated with the damage induced by the energy loss of low energy ions and electrons in the plasma bombarding the sample surface. Between 100 and 240°C proper rectifying properties are achieved with extremely low n-values. The barrier height increases with the temperature up to 240°C. Correspondingly, the H profile broadens starting from the GaAs surface by increasing the substrate temperature, due to the increasing of the H diffusivity, as detected by C-V profiling of the carrier concentration [10]. H likely passivates also electrically active defects in the depletion region, leading to a reduction of the recombination current and contributing to the achievement of almost "ideal" n-values in the temperature range 100-240°C.

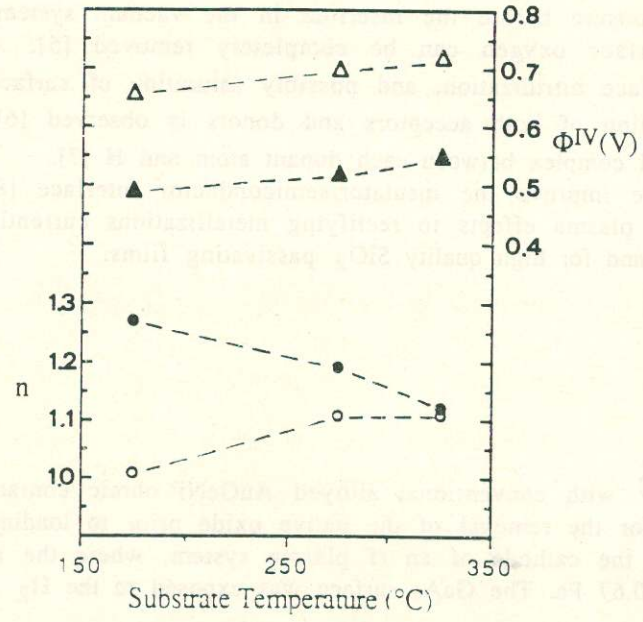

Fig.2. Ideality factor and I-V barrier height for Al diodes as a function of the substrate temperature, for H_2 (open symbols) and $H_2 + N_2$ (filled symbols) plasma treatments.

When H_2 and N_2 plasma treatments are performed at 175°C, low Schottky barrier heights are observed together with degraded n-values, as shown in Fig. 2 for Al dots. The data relative to the H_2 treated Al diodes are reported for comparison, and are similar to those found for Ti/Pt contacts. At higher temperatures an increase of the Φ^{IV} values and decrease of the ideality factors for the $H_2 + N_2$ treated samples are observed but Φ^{IV} is still well below the values relative to H_2. This can be attributed to the cumulative effects of surface damage from the N_2 plasma and GaAs surface nitridization.

By comparing the properties of H_2 and $H_2 + N_2$ treated diodes, we remark that the $H_2 + N_2$ plasma is more detrimental for the diode properties. The differences between the reference HCl cleaned sample and the plasma treated ones decrease by increasing the deposition or annealing temperature, in correlation with the H outdiffusion and the recovery of the plasma induced damage.

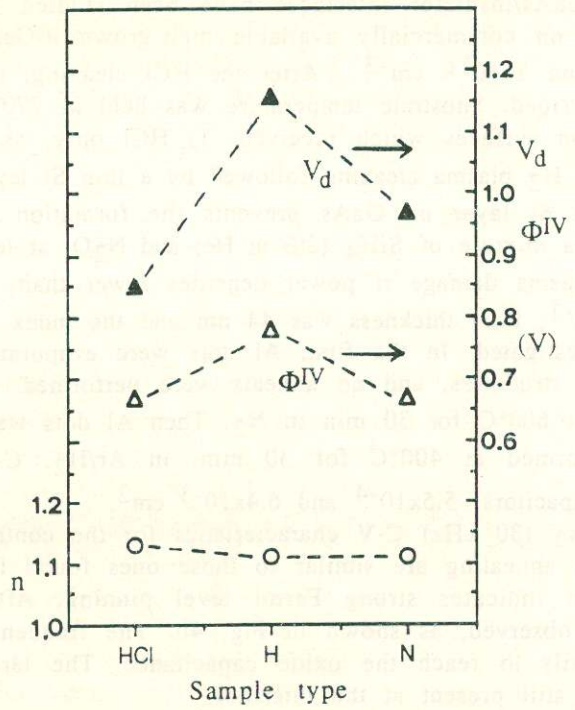

Fig.3. Diode ideality factor n, barrier height Φ^{IV} deduced from the I-V forward characteristics, and diffusion voltage V_d deduced from the C-V data, for WN_x diodes for different surface preparations, annealed at 800°C for 10 min.

2.2 WN_x CONTACTS

Tungsten nitride is a commonly used material for Schottky gates in self-aligned refractory gate GaAs MESFET integrated circuits. In this technology, the gate contact must withstand a high temperature annealing, in the range 800-850°C, needed to activate the n^+ implant in the source and drain regions. In digital integrated GaAs circuits, relatively high diode barrier heights are desirable, to improve the circuit margins. In this work, a WN_x film 200 nm thick has been deposited in-situ by reactive sputtering on HCl (HCl-type samples) only, HCl + H_2 (H-type) plasma, and HCl + H_2 + N_2 (N-type) plasma treated GaAs substrates Si doped at $2x10^{17}$ cm^{-3}. The main parameters of the dc magnetron sputtering deposition were N_2 and Ar flows of 3 sccm and 20 sccm, respectively, pressure of 0.67 Pa, and deposition rate of 0.35 nm/s. The 0.12 mm diameter dots for electrical measurements were defined by photolithographic methods and reactive ion etching in a CF_4-O_2 mixture. The electrical characteristics of the WN_x Schottky diodes were measured before and after annealings at 800°C for 10 min in arsine overpressure.

The as deposited diodes show low Φ^{IV} values and degraded ideality factors, in particular the plasma treated ones, due to the cumulative plasma and sputtering damage. A noticeable recovery of the rectifying properties is observed after high temperature annealings, as shown in Fig. 3. The diode electrical properties are strongly dependent on the GaAs surface pretreatments, even after the 800°C heating. The highest Φ^{IV} values are found for the H-type samples, namely Φ^{IV} = 0.78 V. Lower and similar Φ^{IV} = 0.67 V values are measured for both the HCl and N-type diodes.

Large differences are detected also among the diffusion potential values, V_d, as deduced from C^{-2} - V curves at 1 MHz, and the maximum is found again for the H-type. The large (Φ^{IV} - V_d) difference is commonly found for W-based diodes. This can be attributed to metal/GaAs interfacial states which follow the semiconductor Fermi level under an ac signal, as shown by Callegari et al. [11]. The larger the density of these interfacial states, the higher the (Φ^{IV} - V_d) difference. In the case of the plasma treated diodes annealed at 800°C, however, we cannot rule out the formation of a shallow surface GaAs layer compensated or even p-type, due to minor interfacial interdiffusion processes.

Different electrical properties among the various samples are attributed to different interfacial microreactions, as shown by TEM observations [12]. Such reactions are controlled by the properties of the GaAs surface layer, determined in turn by the surface pretreatments. Thus, the GaAs cleaning procedure can be chosen in order to tailor the Schottky diode properties even after the high temperature heatings, in this case for instance to enhance the Φ^{IV} values.

The WN_x gate fabrication process giving the highest Φ^{IV} values, i.e. the H-type, has been successfully used for self-aligned depletion-mode MESFETs with 1 μm gate lenght. An average Φ^{IV} of 0.76 V has been measured in agreement with the results found for the large circular dots.

3. MOS STRUCTURES

The electrical properties of plasma treated GaAs/insulator interfaces have been studied by using MOS structures. Experiments were carried out on commercially available melt-grown n-GaAs wafers bulk-doped with Si at about $3x10^{17}$ cm^{-3} and $2x10^{16}$ cm^{-3} . After the HCl cleaning, the samples were loaded on an rf cathode previously described. Substrate temperature was held at 270°C in all the experiments. SiO_2 films were deposited on surfaces which received: 1) HCl only, as a control; 2) HCl + H_2 + N_2 plasma cleanings; 3) HCl + H_2 plasma cleaning followed by a thin Si layer deposited in-situ by dc magnetron sputtering. A thin Si layer on GaAs prevents the formation of native oxides [13]. The SiO_2 films were deposited in a mixture of SiH_4 (2% in He) and N_2O, at low pressures ranging from 2.6 to 20 Pa. To minimize plasma damage rf power densities lower than 10 mW cm^{-2} were used, at deposition rates of 4 nm min^{-1}. Film thickness was 44 nm and the index of refraction 1.47. Two types of samples have been investigated. In the first, Al dots were evaporated through a metal mask on the as-deposited SiO_2/GaAs structures, and no anneals were performed. In the second, the SiO_2/GaAs structures were annealed at 600°C for 30 min in N_2. Then Al dots were deposited and a post metallization anneal was performed at 400°C for 30 min. in Ar/H_2. C-V measurements were taken on 2 different area MOS capacitors, $5.5x10^{-4}$ and $6.4x10^{-3}$ cm^2.

The high frequency (1 MHz) and low frequency (30 kHz) C-V characteristics for the control sample are shown in Fig. 4a. The C-V curves before annealing are similar to those ones found for anodic GaAs oxides. The large frequency dispersion indicates strong Fermi level pinning. After annealing, improvement of the C-V characteristics is observed, as shown in Fig. 4b. The frequency dispersion is reduced, but still the 1 MHz curve fails to reach the oxide capacitance. The large hysterisis of about 5 V indicates that slow states are still present at the interface.

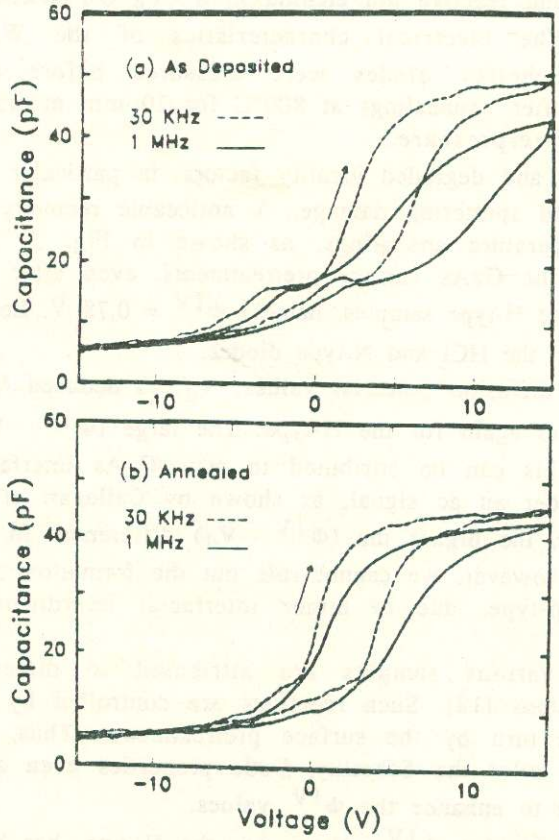

Fig.4. 1 MHz and 30 kHz C-V measurements of a MOS capacitor having had a HCl clean. a) before annealing; b) after annealings at 600 and 400°C.

Fig. 5a shows that improvements in the C-V characteristics occurs in as-deposited samples which received surface nitridation. For this process, it was shown that a nitride first layer is still present at the interface after the dielectric film deposition [5]. The high and low frequency C-V curves still show frequency dispersion. Under negative bias, the capacitance agrees with the inversion capacitance as computed by the Poisson equation. However, quasi-static C-V measurements showed no "dip" indicating that inversion has not been achieved. From the stretching of the C-V characteristics, we conclude that interface states are still present in the gap and therefore the quasi-static dip is not observed.

Fig. 5b shows results for the same MOS sample after annealings at 600 and 400°C. A reduction of the frequency dispersion is observed, but the hysterisis is increased by 2 V when compared with a non-annealed sample. The overall characteristics are slightly better than the control sample of Fig. 4. We suggest that after annealing the nitride layer becomes unstable and reacts with GaAs. This forms As precipitates at the interface, as happens for the oxide layer. The free As is then responsible for the usual pinning effects observed for GaAs.

In the third case, a thin Si layer about 2 nm thick was deposited in-situ on an H_2 treated GaAs surface. An SiO_2 film was then

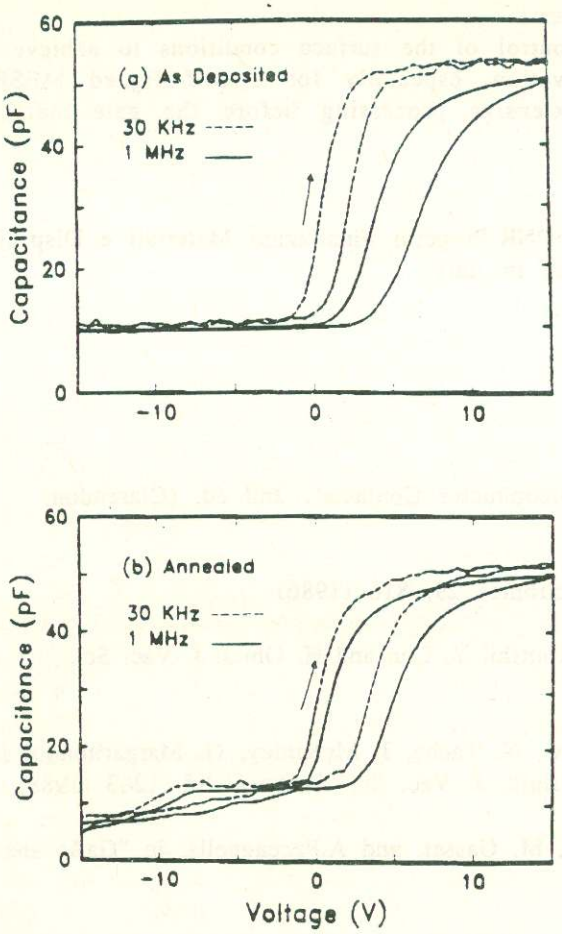

Fig.5. 1 MHz and 30 kHz C-V measurements of a MOS capacitor having had HCl, H_2, and N_2 plasma treatments. a) before annealing; b) after annealings at 600 and 400°C.

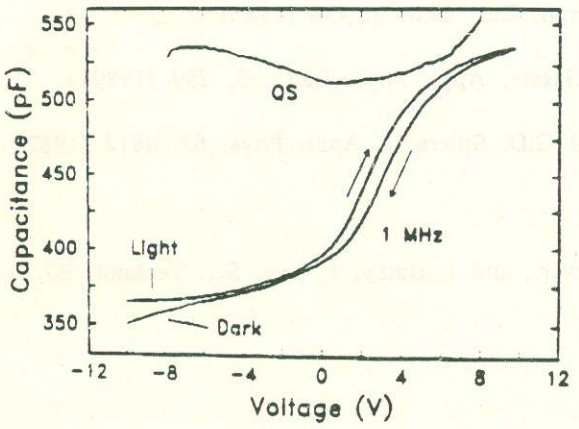

Fig.6. 1 MHz and quasi-static C-V measurements of a MOS capacitor having had HCl, H_2 plasma treatment and a thin Si layer deposited on the GaAs surface, after annealings at 600 and 400°C.

deposited in-situ as described above. The C-V characteristics after the high temperature anneal are reported in Fig. 6. The 1 MHz plot shows that when the voltage goes from positive to negative, the MOS capacitor goes from accumulation to deep depletion under dark condition. If now the device is illuminated, minority carriers are generated and inversion is observed. The stretching of the dip is rather pronounced, in part because the wafers have high doping density ($3x10^{17}$ cm^{-3}) and in part because interface states of the order of 10^{12} cm^{-2} eV^{-1} are still present. The hysterisis is greatly reduced when compared with the standard and the $H_2 + N_2$ treated samples. The low frequency curve is not shown in Fig. 6 to avoid overcrowding. The frequency dispersion is about 3 V.

When thinner Si layers are deposited as a first layer, hysterisis of 2 V were obtained. This hysteretic behaviour was half way between the sample which had 2 nm of Si. Thus, the Si layer has a well defined role at the interface. After annealing, no relevant changes are observed by ellipsometry in the structure. Thus, we can only speculate that the role of the Si layer is in stabilizing the free As at the interface, since native oxides are formed on the as deposited samples.

4. CONCLUSIONS

H_2 and N_2 plasma treatments on the GaAs surface largely modifies the interfacial properties of metal/GaAs and insulator/GaAs systems. At T < 300°C, the Schottky diode characteristics depend on the surface density of H, unannealed plasma induced damage in GaAs, and surface nitridization in H_2 and N_2 treated samples. At high temperatures, T= 800°C, the WN_x diode properties still depend on the GaAs surface cleaning, as different interfacial reconstructions occur depending on the GaAs surface properties. The maximum Φ^{IV} has been found for the H_2 treated samples. In the case of SiO_2/GaAs passivations, when a thin Si layer was deposited first on the GaAs surface, the MOS capacitors could be driven from deep depletion into inversion after the 600°C anneal. Instead, wafers which received surface nitridization were not found to be stable under high temperature anneal, and their C-V characteristics are similar to those found for anodic oxides. These instabilities are interpreted in terms of As cluster

formation due to the decomposition of the nitride layer.

These result underline the need for proper control of the surface conditions to achieve the desired properties of the gate electrode and passivation, especially for a self-aligned MESFET process where the GaAs surface has undergone extensive processing before the gate metal or passivating film deposition.

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