GaAs MMIC BUILDING BLOCKS FOR TV APPLICATIONS

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Abstract :

GaAs MMICs mixers and oscillators have been fabricated for application to VHF-UHF and satellite TV tuners using a 0.7 µm gate length MESFET process available in the Philips Microwave Limeil Foundry, in France. Various mixer configurations have been evaluated which show improved intermodulation/noise figure performance as compared to silicon bipolar circuits. Best circuits have input IP3 over 10 dBm with associated noise figure lower than 10 dB at 2 GHz. The oscillators tested are the multivibrator-type and common gate Clapp differential configurations. Although the fully integrated GaAs VCO's do not meet the phase noise requirements yet, GaAs VCO's coupled to an external hybrid resonator appear however as a good solution to achieve low phase noise wide band VCO's at frequencies higher than 2 GHz.

I - INTRODUCTION

Conventional VHF-UHF and satellite TV tuners are still routinely fabricated using discrete components. Their integration is however highly desirable to decrease the components count and reduce their size. There has been some attempts to integrate direct conversion VHF-UHF tuners using a Si-process (1), and more recently GaAs technology has been used to demonstrate the feasibility of a double conversion VHF-UHF tuner (2) and that of satellite TV tuners (3-4). The integration however cannot succeed if the performance does not reach at least that of hybrid circuits. This means that careful investigation of each building block of a tuner is required to achieve the best performance. In this paper, we present a study of GaAs mixers and oscillators IC's for application either into a double frequency conversion VHF-UHF tuner or a satellite TV tuner (950 MHz - 2 GHz). The ICs have been fabricated using the D07A GaAs process available in the Philips Microwave Foundry in Limeil, France. It is a depletion mode MESFET process with Vt = - 3 V, Idss = 300 mA/mm.

II - MIXERS IC's

2.1. - Design

All the mixers are double balanced because of some advantages which make them more interesting than single ended ones for integration :

a) virtual grounding, which strongly reduces sensitivity to ground inductances and also minimizes spurious signals into bias lines and ground,

b) better LO to IF and LO to RF isolation because LO signals cancel at the RF and IF ports in double balanced mixers.

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The basic mixer consists in four transistors as shown in figure 1. On that basis, various mixers have been designed with different RF input stages, IF output stages. Input stages studied are common source, common gate and differential amplifier. In the last version (figure 2), the effect of a series feedback resistor Rs on noise figure and intermodulation has been investigated. The output circuit is either a resistor with symmetrical output via 50 ohms buffers, or a transformer tuned to the desired IF frequency.
This last solution strongly reduces the power dissipation (no buffer) but requires external components. The size of the transistors is also a parameter which has been varied in some structures to study its effect on mixer performance.

2.2. - Measurements

As the mixers are double balanced, hybrids have been required to split the RF and LO powers into balanced signals. Similarly, an hybrid has been used to add the IF powers in the mixers that provide symmetrical buffered outputs. For that reason, the input and output powers which are talked about must be defined clearly. In what follows, the RF and LO powers are referred to the input of hybrid splitters and the IF power, to the output of the hybrid combiner when used.

The table 1 compares the typical performance of 3 mixers with common source RF input, buffered outputs, using a resistor as IF load. The IF frequency is 100 MHz and RF is 2 GHz.

The input IP3 reaches 15 dBm with the DBM 3SB version with an associated noise figure of 12.5 dB when LO power is 16 dBm. By increasing the size of the RF transistor to 200 µm (DBM1SB) instead of 100 µm, the conversion gain improves as well as the noise figure at the expense however of a lower IP3. By increasing the mixer size (DBM2SB) while keeping the RF to LO transistor size ratio equal to 2 as in the DBM1SB mixer, the noise figure improves by about 1.5 dB with similar gain and input IP3. No significant variation in mixers performance has been observed when increasing the IF frequency up to 500 MHz or decreasing the RF frequency down to 1 GHz.

It is also interesting to compare mixers with buffered output to mixers with a transformer as output stage. The table 1 reports the performance of DBM1S mixer at IF = 480 MHz. The conversion gain is lower than in the buffered version because the transformer does not provide power gain, but the noise figure is better. The input IP3 however is lower and is about 9 to 10 dBm. The reason is not very clear at now but we expect this is due to a difference in the IF load impedance to the basic mixer. With a transformer, the load impedance is roughly equal to the output impedance of the basic mixer, while it is lower in the buffered version. Consequently, the IF voltage swing on the drain of the LO transistor is lower in the buffered mixers, and this is probably the reason for a better IP3.

In the figure 3 is shown the performance of mixers with differential RF input amplifiers as a function of the series resistance value Rs. The input IP3 increases when increasing the value of Rs, roughly by the same amount as the noise figure, and also roughly by the same amount as the gain decreases. This means that up to a few dBs of gain reduction, the series resistor has nearly the same effect as an attenuator in front of the mixer. Consequently, the noise figure/intermodulation performance of the mixer is not improved but the use of a series resistor can be interesting to achieve a desired IP3 performance.

Some mixers have not yet been tested such as common gate input mixers but we hope that more complete results will be available at the time of the conference.

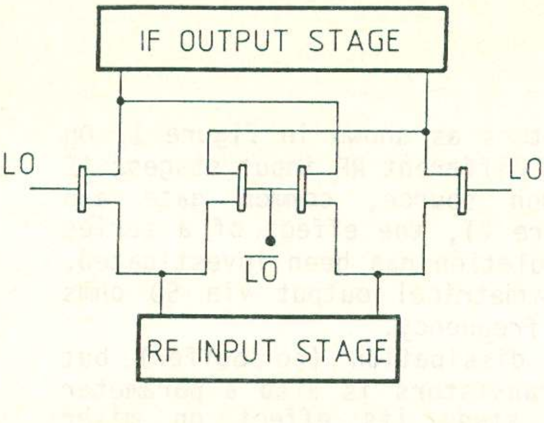

Figure 1
Basic mixer configuration

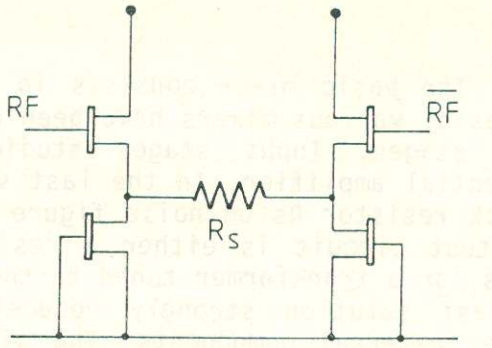

Figure 2
Differential RF input stage with series feedback

MIXER	DBM1SB	DBM2SB	DBM3SB	DBM1S
IF load	resistor + buffer			transformer
IF freq.	100 MHz			480 MHz
LO/RF FET size (um)	100/200	240/480	100/100	100/200
Gain (dB)	2/3.5	1.5/3	0.5/2	-1/0.5
NF (dB)	12/10.5	10.5/9	14/12.5	10.5/9
input IP3 (dBm)	11/13	11/12.5	13/15	9/10
consumption (mA)	10 (+40)	25 (+40)	10 (+40)	10

Table 1
Mixers performances at 2 GHz
The two figures correspond respectively to LO power of 13 and 16 dBm

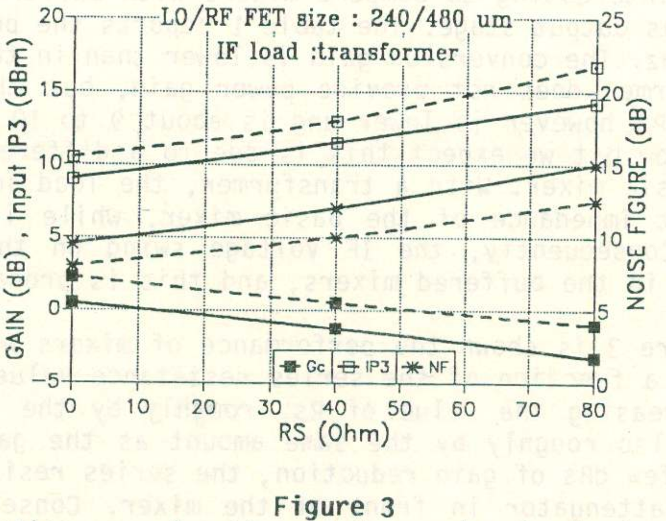

Figure 3
Mixers characteristics as a function of the series feedback resistor value Rs
——— LO = 13 dBm ; - - - LO = 16 dBm

II - OSCILLATORS IC's

3.1. - Design

The oscillator is may be the most difficult part to design in a TV receiver because of the wide bandwidth and low phase noise specifications which are to be met simultaneously. In addition, there is almost no design tool able to predict the phase noise of an oscillator, therefore "try and see" is still the best design technique. The maximum phase noise acceptable is not well-known but is probably around - 90 dBc/Hz at 100 kHz offset assuming a $1/f^3$ decrease of the phase noise with offset frequency.

Two basic oscillators have been designed that deliver balanced output signals as required for driving the mixers. The first one is a multivibrator-like oscillator (fig. 4) and the second one is a grounded gate Clapp oscillator (fig. 5). These oscillators have been designed to be connected to an external tank circuit but two fully integrated versions of the Clapp oscillator have also been fabricated (fig. 5b). One is a 2.3 GHz fixed frequency oscillator and the other is a broadband VCO designed for application into a double frequency conversion VHF-UHF TV tuner (fig. 6).

3.2. - Measurements

The phase noise of the integrated 2.3 GHz Clapp oscillator is very low and equal to - 103 dBc/Hz at 100 kHz offset. It decreases as $1/f^3$ up to a few hundred kHz offset frequency as shown in fig. 7. The integrated VCO version has been obtained by replacing the Css MIM capacitor by a planar Schottky varicap. This enables to cover a very wide band, from 2.3 GHz up to 3.6 GHz. The phase noise is however degraded by at least 12 dB as compared to the fixed oscillator and lies between - 91 and - 78 dBc at 100 kHz offset (fig. 7). Such a degradation may have several origins :

a) Diminution of the quality factor due to the series resistance of the varicap. This effect explains certainly a great part of the high phase noise oberved at 3.3 GHz where the varicap is biased around pinch-off voltage and has a very low Q (5). However, we do not expect this effect to be responsible for more than 2 or 3 dB phase noise increase at the lower and upper ends of the frequency range.

b) Non-linearity of the varicap leading to conversion of 1/f low frequency noise into phase noise.

c) additionnal 1/f noise generated into the varicap converted into phase noise.

We don't know at now which of the last two causes is the main one but CAD tools are being developed that should indicate how varicaps contribute to phase noise. The above results show however that the phase noise of broadband integrated VCOs is still too high, but the limit of - 90 dBc does not seem to be out of reach. Better phase noise can be expected using an external resonator, because of higher Q factors of inductances and because the above mentioned b) and c) contributions are probably lower with Si-varicaps. The connection to an external tank circuit is not easy however from a practical point of view. We tried using SMD components outside the package in which the chip VCO's was mounted, and we succeeded to make it oscillate at frequencies higher than 2 GHz quite easily, but we could not cover a very wide band (600 MHz maximum) probably because of parasitics capacitances. In these conditions, a comparison with the integrated VCO is not easy, because of different structure and bandwidth, but there seems to be nevertheless an improvement in using an external tank circuit since the maximum phase noise observed was about -90 dBc/Hz at 100 kHz offset. In all cases, the phase noise improved when increasing the varicap bias voltage. At high bias voltage ($\gg$20 V), the phase noise was typically lower than - 100 dBc/Hz either with the multivibrator or Clapp VCO's. The figure 8 shows an example of spectrum obtained with a Clapp VCO's connected to an external tank circuit.

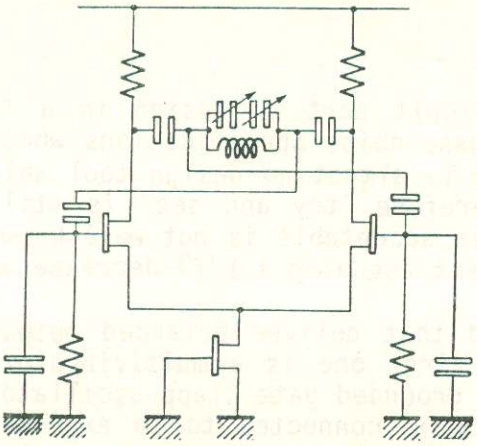

Figure 4
Multivibrator oscillator coupled to an external resonator

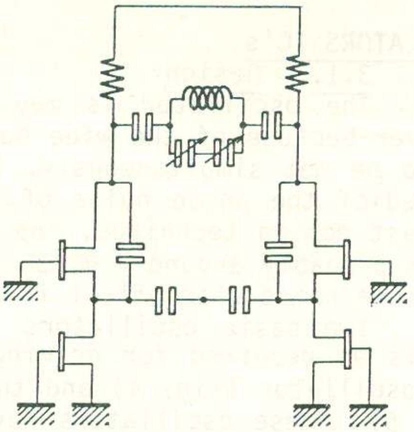

Figure 5a
Grounded gate Clapp oscillator coupled to an external resonator

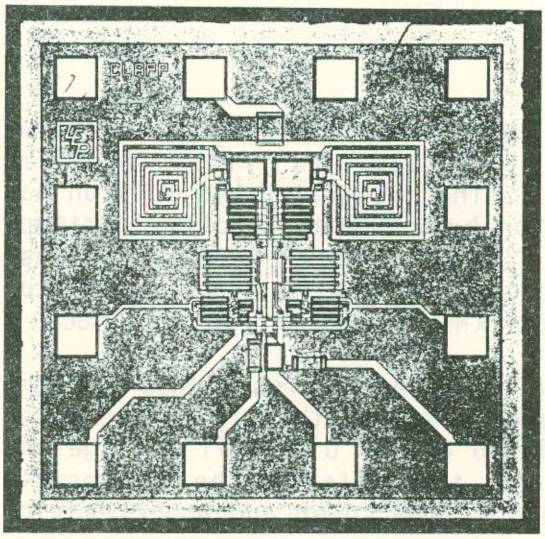

Figure 6
Photography of the integrated Clapp VCO

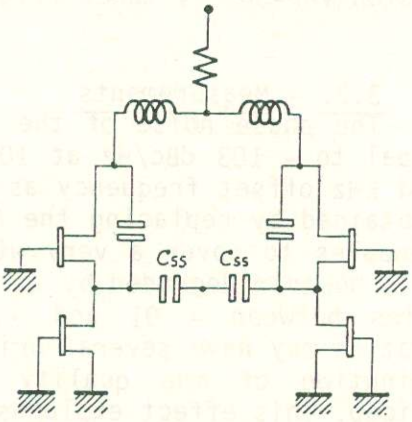

Figure 5b
Full integrated Clapp oscillator
The Css capacitance is a varicap in the VCO version

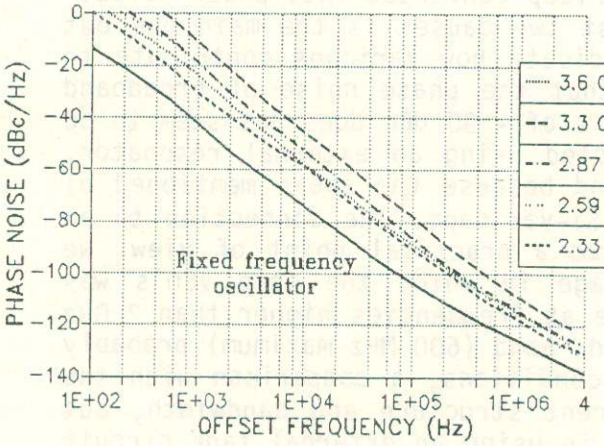

Figure 7
Phase noise of integrated Clapp oscillators

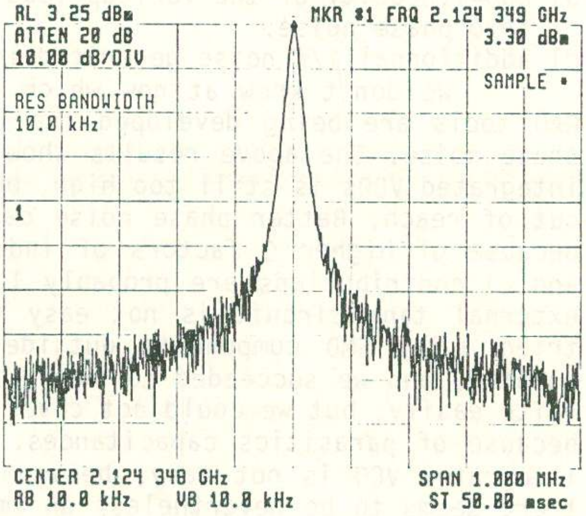

Figure 8
Oscillation spectrum of a Clapp oscillator coupled to an external resonator

IV - CONCLUSION

We have shown that GaAs mixer/oscillator IC's fabricated using a commercially available process offer attractive performance for TV application, particularly in the satellite TV band which cannot be covered with good performance using current Si bipolar processes.

Acknowledgements

The authors would like to thank Mr. J. van Bruggen from the Philips Components Application Laboratory, Eindhoven for his helpfull advices given during this work and the Philips Microwave Limeil Foundry staff for there efficient and fast processing.

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