AN EXPERIMENTALLY BASED SYSTEMATIC APPROACH FOR YIELD AND RELIABILITY EVALUATION IN GaAs MMICs

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Abstract

After a critical examination of the state of the art yield and reliability evaluation tools, the results are reported of a systematic experimental analysis for the MMIC yield evaluation. The possibility is then proved of determining efficient MMIC reliability evaluation rules. Finally, the main features and the results until now obtained will be reported for an experimental reliability program aimed at giving the Telettra designers the relevant data base.

Introduction

The recent years have shown an impressive increase of the GaAs MMIC research efforts and a noticeable deepening of a number of technical problems posed from their high quality producibility. This special scientific and industrial interest is ascribable to well known advantages of MMICs over more conventional microwave circuits such as higher potential reliability, lower sizes, reduced costs (especially for high volumes), inherent wide band performances and capability of doing logic and analogic functions on the same chip. These advantages raised the enthusiasm of the microwave community to such a point that many GaAs foundries were created for customer designed MMIC production.
In spite of this success the MMIC yield and reliability have not sufficiently deepened for giving the designer means adequate to their correct evaluation in a given circuit topology. Various more or less questionable approaches [1,2,3] have been proposed but a basic background of criteria, suggestions and recommendations is, at present, lacking.
In this paper the main features and the results until now achieved will be described for a systematic experimental research effort performed at Telettra SpA and aimed at giving a full solution to the above problems.
More in detail the paper will:

a) Syntetically describe and critically analyze the state of the art yield and reliability evaluation tools.
b) Report and discuss the experimental results of a systematic yield evaluation analysis we performed on a wide number of single MMIC circuit elements.
c) Prove the possibility of defining adequate reliability evaluation criteria for properly designed MMICs.
d) Describe the main features and the results until now obtained of an experimentally based reliability evaluation program aimed at giving the Telettra designers the relevant information and data base.
e) Draw, on the basis of the above points, a number of practical suggestions and recommendations for foundry customers.

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Yield evaluation

The total yield Yt of a given MMIC circuit topology can be written as a product of single process step yields:

$$Yt = Yl*Ydc*YP*Yb*Ya$$

where: Yl (line yield) is the fraction of wafers which completes the fabrication process unbroken and with acceptable process control monitor (PCM) parameters. This yield is a function of the overall process maturity and reliability, so that it can be considered as an useful parameter for evaluating the adequacy level of the used technology.
Ydc (functional yield) is the fraction of on wafer MMIC chips which passes a full d.c. probing. Yp (parametric yield) is the fraction of chip which have passed the d.c. test and meet the r.f. performances specifications. Yb (dicing yield) is the good r.f. chip fraction which survive to the wafer dicing. Ya (assembling yield) is the well diced chip fraction correctly operating after the assembly operations.
The Yl value depends on the PCM parameter acceptance ranges, a reference set of which (Telettra 0.5um process) is reported in Table I. Such ranges very favourably compare with those used in various GaAs foundries [8]. Reasonably good Yl values, using Table I data, must be >75%.
For a given MMIC circuit, the functional yield Ydc depends on the topology complexity because its value is given by the product of the d.c. yields of each circuit element. The simplest way to evaluate Ydc is to define [3,4] a mena yield for each circuit element. In Table II the mean single component d.c. yields used at Anadigics foundry are reported.
This evaluation system cannot be considered as fully satisfactory [8], because the d.c. yield of components like FETs, diodes and capacitora depends on their size. On the other hand our MMIC development experience has demonstrated that the circuit elements more critical in determining the MMIC d.c. yield are FET devices (single or dual), MIM capacitors and via holes. The other circuit element yield is usually so high that a size independent mean yield can be defined without introducing relevant errors in the overall Ydc calculation. Some foundries take into account the effect of these elements by defining a d.c. yield factor per unit chip area [8].
For FETs the definition of yield per unit gate width has proven to be, unless for our experience, more realistic. A similar concept applies to MIM capacitors where yield per unit capacitance is correctly defined. For vias, the definition of a yield per via is adequate.
An useful instrument for foundry customers is the merit classification [8] for MMIC single element d.c. yields, given in Table III.
The parametric yield Yp evaluation requires Monte Carlo calculations (easily available on the standard circuit simulation computer programs) based on the fluctuations of the individual element equivalent circuit parameters. Typical parameter fluctuations for the Telettra 0.5/um FET technology are shown in Tables IV and V.
The Yp calculations usually assume mutually uncorrelated parameter fluctuations (5) so that their are normally quite far from reality. A more realistic approach should take into account as mutually uncorrelated parameters a set of basic processing fluctuating parameters as, for example, the doping profile, the gate length, the recess depth, the ohmic contact resistance etc. This idea was originally proposed by Ladbrooke (6) and extensive work is being actually done at Telettra to make the related computer programs and experimental supporting data available.

In order to obtain yield levels reasonably high with respect to the wordl-wide state of the art, a very important recommendation for the designer which has to chose and use external foundry services is to control how favourably the individual circuit element yields compare with the data of Table III. Similary Tables IV and V can be used as a reference for evaluating the adequacy of the single circuit element reproducibility.
Table VI gives single element d.c. yields as obtained at Telettra. They were obtained by averaging the results of 5 groups of 100 identical elements for each type of circuit elements. For example, for the single gate FET, 5 groups of 100 elements having 150,300,600,1200 and 1400 μm gate width respectively were tested. A reasonable value for Y_D (chip area $\leq 4 \times 4\ m^2$) must be $\geq 95\%$, similary for Y_A (circuit with ≤ 16 pads) must be $\geq 95\%$.

MMIC reliability evaluation

The reliability of hybrid circuits is well established and based over a long circuit development and testing experience. It can be easily calculated by applying a well known additive failure rate formula [7]. On the other hand, as previously outlined, a well defined procedure to calculate the expected reliability parameters of a given GaAs MMIC circuit topology is, at present missing. For this reason some [1,2] of the first papers (1987) in the MMIC reliability field, even if written by people well experienced in the MMIC design, used the above mentioned additive procedure. Unfortunately the validity of such an approach has not been confirmed by a number of life test experiments [9,10] on logic GaAs ICs, which have shown mean life values much higher than those obtained by the additive approach. An extensive critical work [8] recently performed, has outlined, for MMIC circuits which have been designed following well defined rules (also detailed in [8]), the following important features:

a) The single MMIC circuit element having the shortest life time and substantially determining the MMIC life time, is the FET device.
b) The primary MMIC failure mechanisms and the relevant activation energies (usually between 1.4 and 1.8 eV) are the same of the single FET devices, the overall life time being in most cases of the same order of magnitude. Such primary failure mechanisms are ascribable to the a thermally activated Au-GaAs interdiffusion either in Schottky gates or in ohmic contacts.

The above points show the possibility of giving the designer practical means for evaluating the expected reliability of a given MMIC circuit topology.
In order to make available the required data base, a systematic reliability evaluation program has recently started in Telettra. The program was generated by on ESA/ESTEC contract (no.714/88/NL/JG) and is aimed at correlating the reliability of the 4-8 GHz MMIC amplifier shown in Figure 1, with that of its circuit elements.
The program is organized in three phases, which can be summarized as follows.
Step stress measurements (both thermal and electrical) must be first done on a number of single circuit elements constructed in the PCM pattern of the amplifier fabrication process (phase 1) with the purpose of determining the optimal conditions for subsequent life time tests. Then, life time measurements must by performed both on PCM circuit elements (phase 2) and on the full MMIC. Further details on the performed experiments and the relevant results will be given in the oral presentation.

Conclusions

The state of the art yield and reliability evaluation tools have been critically analyzed. The results of a systematic yield evaluation experimental analysis have been reported. The possibility of determining reasonable reliability evaluation rules for correctly designed MMIC circuit has been established. The main features of an experimental reliability program aimed at giving the Telettra designers the required data base have been described.

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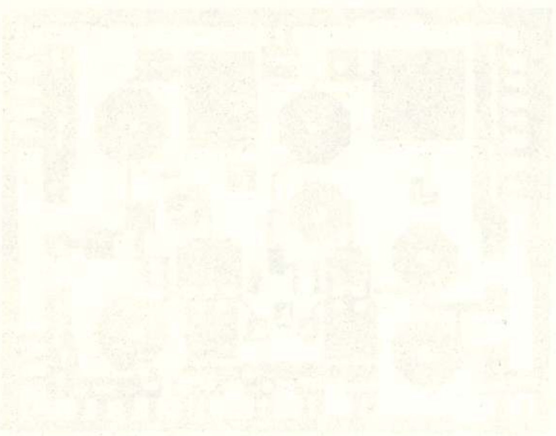

PARAMETRI	
I_{dss}	± 15
g_m	± 15
V_p	± 20
C_{gs}	± 20
RN	± 20
RN^+	± 10
R_{metal}	± 10
C (MIM)	± 10

Table I - Acceptable range of PCM parameters for 0.5/um ion implated technology

Component	Yield
Single gate FET (1/um and 0.5/um gate length)	.950
Dual gate FET (1/um and 0.5/um gate length)	.930
Via holes	.950
Air bridges	.999
Spiral inductors	.990
Interdigitated capacitors	.999
MIM capacitors	.999
Distributed elements	.9999
Active layer resistors	.990
Thin film metal resistors	.999
Schottky diodes	

Table II - Typical mean functional yield data for each single circuit component given by Anadigics Inc.foundry.

	Very good	Good	Acceptable	Unsufcient	Unacceptable
Single Gate FET (1/um gate length, 1 mm gate width)	>.90	.90 -.80	.80 -.60	.60-.40	<.40
Single Gate (0.5/um gate length, 1 mm gate width)	>.72	.72 -.64	.64 -.48	.48-.30	<.30
Dual Gate FET (1/um gate length, 1 mm gate width)	>.81	.85 -.70	.70 -.50	.50-.30	<.30
Via holes (per via)	>.96	.96 -.85	.85 -.80	.80-.70	<.70
Air Bridges (per bridge)	>.995	.995-.98	.98 -.90	.95-.90	<.9
Spiral Inductors (planar type)	>.99	.99 -.98	.98 -.95	.95 -.90	<.9
Interdigitated Capacitors	>.995	.995-.99	.99 -.98	.98 -.95	<.95
MIM Capacitors (1 pF,0.5/um Si_3N_4) (per pF)	>.97	.97 -.94	.94 -.9	.9 -.8	<.8
Distributed Elements	>.998	.998-995	.995-.85	.985-.97	<.97
Active layer Resistors	>.98	.98 -.90	.90 -.80	.80 -.70	<.70
Thin film metal resistors	>.995	.995-.98	.98 -.95	.95 -.90	<.9
Schottky Diodes (area 10-100/um^2)	>.87	.87 -.85	.85 -.75	.75 -.60	<.60

Table III - Merit evaluation for the functional yields of various circuit elements.

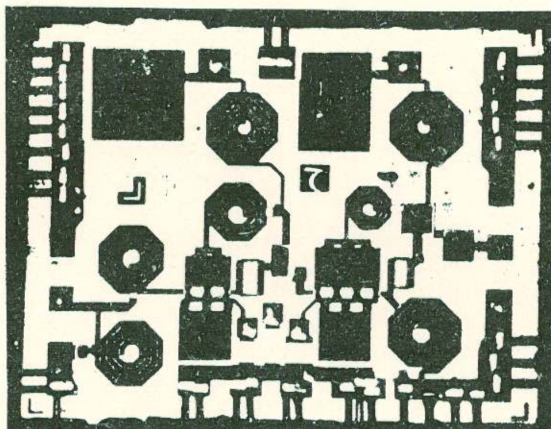

Fig.1 - The test MMIC circuit.

PARAMETERS	SYMBOL	
Saturation current	I_{dss}	5%
Transconductance	G_m	3%
Pinch-off voltage	V_p	5%
Gate-to-source-capacitance	Cg_s	10%
Gate-to-drain capacitance	Cg_s	10%
Drain-to-source capacitance	Cd_s	5%
Input resistance	R_I	5%
Drain-to-source resistance	Rd_s	10%
Source resistance	R_s	10%
MIM capacitance per unit area	C_m	5%
N^- layer sheet resistance	R^-	5%
N^+ layer sheet resistance	R^+	10%
Thin film resistors resistance	R_F	5%

Table IV - On wafer typical standard deviations of the single element equivalent circuit parameters for the 0.5/um Telettra MMIC technology.

PARAMETERS	SYMBOL	
Saturation current	I_{dss}	5%
Transconductance	G_m	5%
Pinch-off voltage	V_p	8%
Gate-to-source-capacitance	Cg_s	10%
Gate-to-drain capacitance	Cg_d	10%
Drain-to-source capacitance	Cd_s	5%
Input resistance	R_I	20%
Drain-to-source resistance	Rd_s	20%
Source resistance	R_s	15%
MIM capacitance per unit area	C_m	5%
N^- layer sheet resistance	R^-	5%
N^+ layer sheet resistance	R^+	10%
Thin film resistors resistance	R_F	10%

Table V - Wafer to wafer typical standard deviations of single element equivalent circuit parameters for the 0.5/um Telettra MMIC technology.

Single Gate FET (1/um gate length, 1 mm gate width)	0.8
Single Gate (0.5/um gate length, 1 mm gate width)	0.6
Dual Gate FET (1/um gate length, 1 mm gate width)	0.7
Via holes (per via)	0.8
Air Bridges (per bridge)	0.98
Spiral Inductors (planar type)	0.99
Interdigitated Capacitors	0.92
MIM Capacitors (1 pF, 0.5/um Si_3N_4) (per pF)	0.99
Distributed Elements	0.99
Active layer Resistors	0.9
Thin film metal resistors	----
Schottky Diodes (area 10-100/um^2)	0.85

Table VI - Single element dc yield values of Telettra MMIC technology.