PRODUCTION CONSIDERATIONS FOR GaAs MMICs

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ABSTRACT

Techniques have been studied to enhance the yield of circuits from a fixed, commercially available GaAs MMIC Foundry process and also to facilitate system implementation of the circuits. Three approaches to yield enhancement have been evaluated using an S/C band amplifier and the results are presented. A modified version of the circuit, configured to operate from a single, low-current bias supply, is also described.

INTRODUCTION

Yield has two main aspects, those of design yield and production yield. This work assumes an established circuit design and the paper will concentrate on long term production yield from a fixed process. To enhance the production yield at this stage it is necessary to increase the number of devices produced to specification. This has been approached in two ways: (i) recouping performance lost due to excursions of device performance as a result of process variation, and (ii) reducing chip area to increase the number of sites per wafer.

(i) The first approach requires that established designs may have to be changed to recover marginal performance. Any technique which involves process modification must be examined carefully, and done as simply as possible, so that an already good process yield is not impaired.

(ii) Generally, as chip size decreases the yield (defined as the number of RF-working chips) is increased. Therefore, a considerable library of techniques is required to reduce the size of a given circuit within the rules and capability of the process. By the definition, prototyping and application of these techniques we have been able to reduce the chip size by 50%, whilst attaining equivalent performance.

Excursions of device performance have been diagnosed at the earliest possible process stage by RFOW evaluation of the FETs before most of the passive elements are defined. This mid process RFOW assessment was used extensively, along with CAD modelling, to predict final circuit performance. With these data various circuit techniques were used to regain the required circuit performance. These techniques included mask selection and electronic tuning.

Having established and proved these two categories of yield enhancement technique, another technique was evolved and demonstrated which greatly reduces the bias supply problem presented to the system designer. By the use of direct current recycling and self bias techniques the production amplifier may be biased from a single 12V supply.

Therefore the production considerations of both cost per function and ease of biasing are addressed, and solutions to these problems demonstrated over a number of wafers by the use of both traditional and novel RFOW techniques.

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TECHNOLOGY

The terms of reference for the study were that a standard Foundry process was to be used. This was the Plessey F20 process, which has 0.5μm gates, through-GaAs vias and an interconnect metallisation supported by multiple dielectric passivation layers. The repeatability of this already high-yielding process ensured that variations in passive elements were not the principal yield determining factor. Variation in FET parameters was identified as being significant. In addition, RF failure is found to affect an entire wafer, rather than individual devices. Therefore at C-Band, techniques of mask substitution rather than those that alter the performance of individual chips are relevant. Laser trimming, valid for individual chips, is of little use for a production process where whole wafers fail.

A diagnostic method to determine whether a particular wafer had high or low parasitic capacitances was therefore needed, and found in mid-process RF on-wafer (RFOW) assessment. Experimentation demonstrated difficulties in making good electrical contact for mid-process RFOW to the thin first level metallisations of the GaAs devices. A process modification was therefore introduced whereby the upper-level metallisation (M3) of a calibration cell was patterned, for RFOW purposes, before the remaining circuits. The upper-level metallisation pattern for these circuits could be chosen from a range of similar photomasks in order to maximise the final circuit RF yield, the mask selection being based upon the RFOW performance of the test cells.

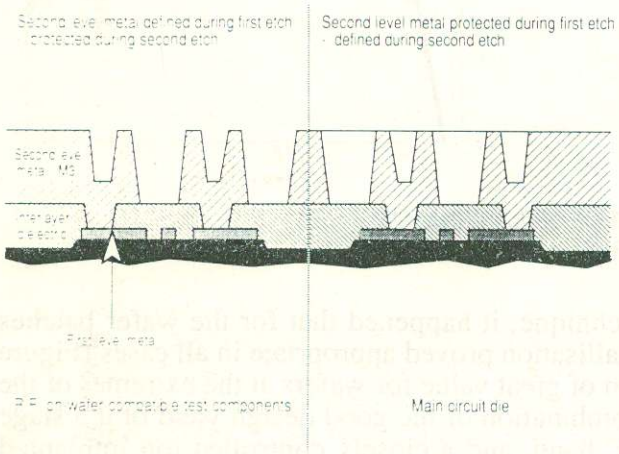


Figure 1 SELECTABLE M3 PROCESS FOR MID-PROCESS RFOW MEASUREMENT OF TEST FETS

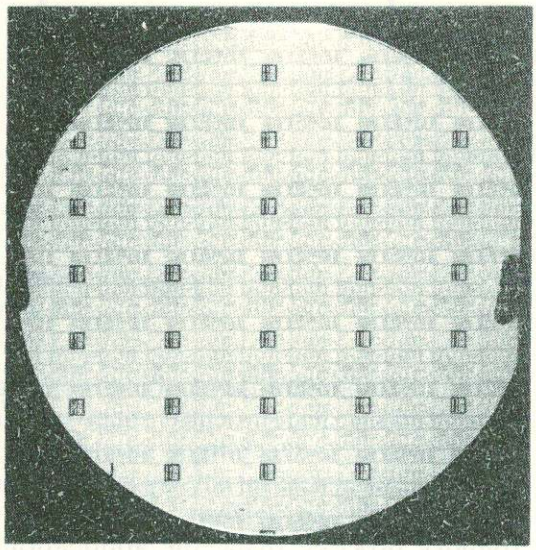


Figure 2 COMPLETE WAFER AT MID-PROCESS. RFOW TEST CELLS ARE CLEARLY VISIBLE

A cross-section of the process is shown in Figure 1. A view of a complete wafer at mid-process is shown in Figure 2 with details of the test cell in Figure 3. This cell permits on-wafer calibration and measurement of the test FETs. The S-parameters can then be inserted into the original design program and one of a number of top level masks selected. The top level metal is the most versatile layer in the process and masks can be designed for different electrical lengths in distributed circuits, or, as applied here, to select different values from multi-contact feedback resistors to provide gain and noise slope compensation. The predicted performance of the alternative M3 patterns is shown in Figure 4. In order to provide a simultaneous comparison, the alternative M3 patterns were laid out on the same demonstrator array. The performance and repeatability of the RFOW results are shown in Figure 5.

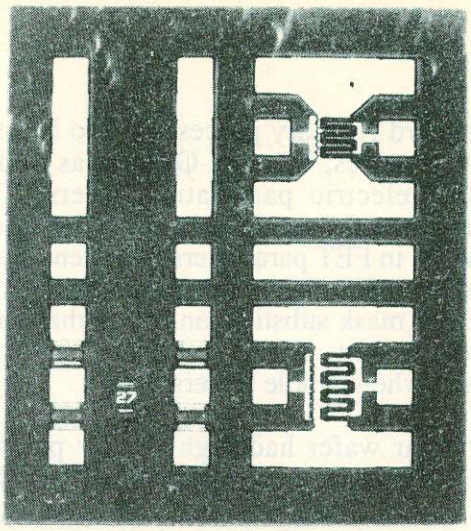


Figure 3 RFOW TEST FET CELL AT MID-PROCESS

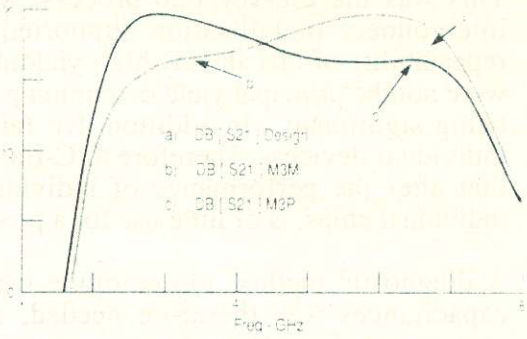


Figure 4 PREDICTED PERFORMANCE OF ALTERNATIVE M3 SELECTIONS

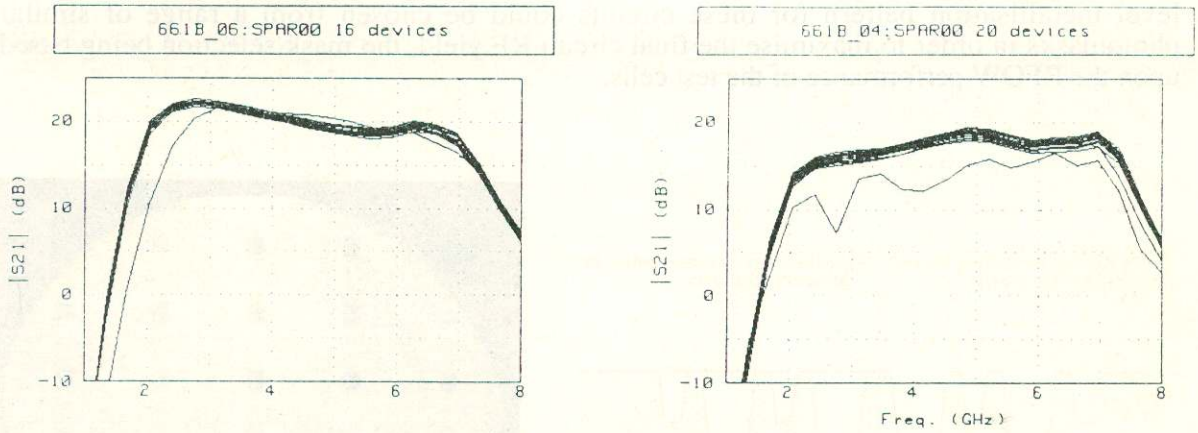


Figure 5 PERFORMANCE OF ALTERNATIVE M3 PATTERNS

Having established this to be a working technique, it happened that for the wafer batches processed the design-centre upper-level metallisation proved appropriate in all cases (Figure 6). However, the technique would have been of great value for wafers at the extremes of the allowed implanted resistivity range. The combination of the good design yield of a 3 stage LNA, which had performance in hand at C band, and a closely controlled ion implanted foundry process, made the application of such a powerful technique unnecessary. The benchmark was also used to evaluate the examples of yield enhancement technique described below which did not require any change to the foundry process, or additional measurement.

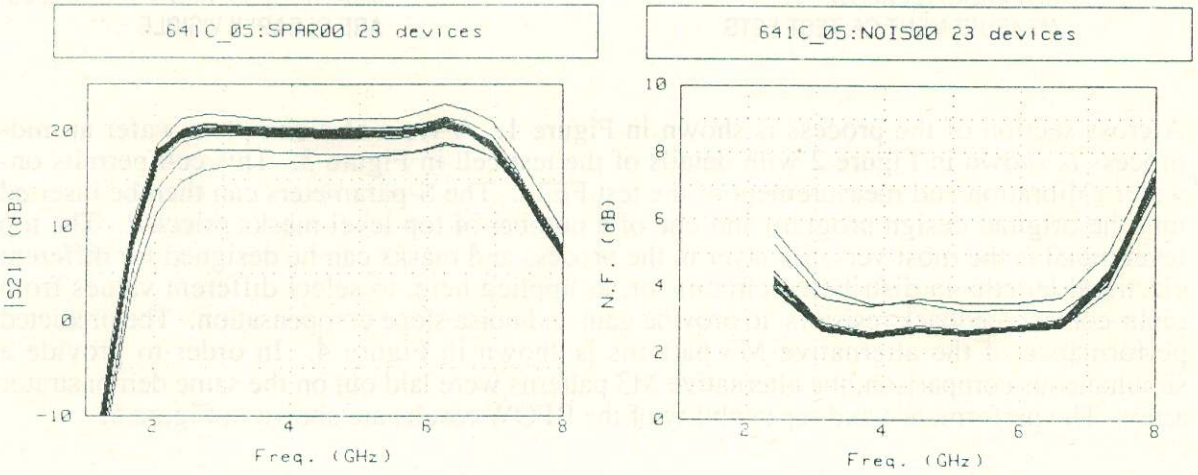
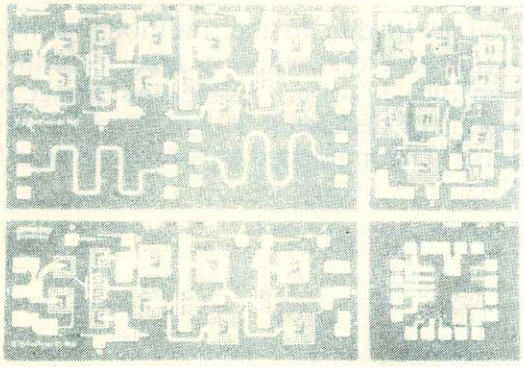


Figure 6 MEASURED PERFORMANCE OF BENCHMARK LNA

An alternative approach to marginal performance recovery was evaluated using voltage variable resistors (varistors) in place of the feedback resistors. This technique, however, requires additional circuit area and, as shown in the results below, the presence of additional active devices has a deleterious effect on the yield.

DESIGN FOR YIELD

Cost per unit circuit function may be substantially decreased by increasing the number of chips per wafer. The techniques required to compress the topology while retaining commercial performance will vary with the foundry chosen. The original circuit and compressed topology circuit are both shown in Figure 7. Some of the important techniques relevant to the Plessey Foundry at C band are briefly described: (i) RF chokes are replaced with overlay spirals, (ii) single turn accurately designed source inductors replace multiple spirals, (iii) common through-GaAs vias shared between two stages of the circuit, (iv) smaller FETs, which are the smallest that obey the minimum interlayer via rule of the Foundry, are used. This last objective resulted in 6 x 100µm replacing the original 8 x 75µm FETs. Criteria applied throughout were to use a circuit with performance in hand and use standard components and techniques as much as possible, against a background of trend plots accumulated over a large number of wafers using the process control monitor (shown in Figure 7).



C Band LNA with tapped feedback resistors	Compressed topology LNA
C Band bench mark	Process control monitor

Figure 7 A QUADRANT OF THE DEMONSTRATOR ARRAY OF CIRCUITS

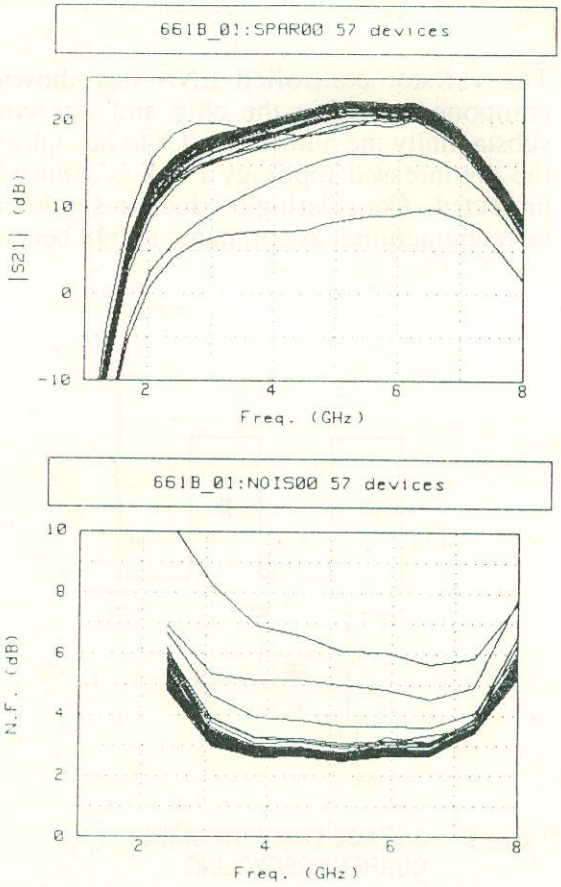


Figure 8 PERFORMANCE OF REDUCED AREA LNA

RESULTS

The performance of 57 compressed topology LNAs from a single wafer is shown in Figure 8. It is clearly seen that there is a gain slope. This is because the 6 x 100µm minimum geometry FETs have higher f_T and lower parasitic capacitances, C_{gs}/C_{gd}, than the benchmark 8 x 75µm FETs. The resulting gain slope may itself be compensated for, by adjustment of the feedback resistors.

Table 1 shows yield, measured by RFOW over 5 wafers for the compressed topology LNA, the three larger LNAs and the varistor controlled LNA. It is interesting to note that as a percentage value of total chips the yield of the benchmark is 61% and of the compressed topology LNA is 54%. This is thought to be due to the fact that for a given arbitrary defect density the more compressed topology is more susceptible to failure. Another point to note is that the area of the compressed topology amplifier is 64% of the benchmark. It could have been reduced to 50% but was designed slightly larger to investigate additional techniques.

Table 1: Circuit Yield Summary from 5 Wafers

Circuit	Tested	DC Pass	DC Yield	RF Pass	RF/DC Yield	Overall Yield	Area (mm^2)	RF Working per 2" wfr	RF Working per 3" wfr
Reduced Area LNA	436	287	66%	234	82%	54%	2.79	342	771
Full Size LNA	423	288	68%	259	90%	61%	4.34	244	548
Varistor Controlled LNA	138	93	67%	74	80%	54%	5.33	170	383

The varistor controlled LNA has shown a reduced yield due to the additional active components within the chip and this combines with the increased chip area to reduce substantially the number of ICs to be expected from a dedicated wafer. The real advantage of the compressed topology LNA is seen when the yields of dedicated 2" and 3" slices are projected. Considering production single-circuit masks, 771 compressed topology LNAs will be manufactured, as compared to 548 benchmark LNAs.

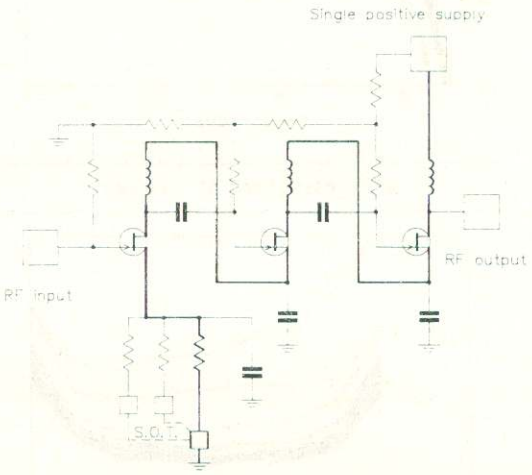


Figure 9 3-STAGE LNA WITH DIRECT CURRENT RECYCLING

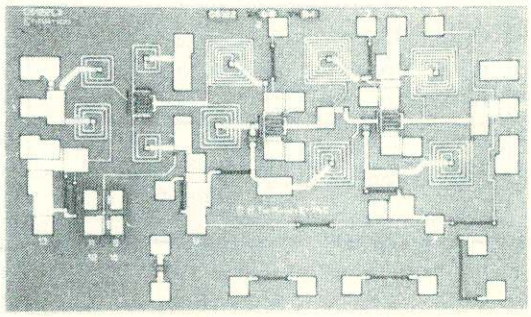


Figure 10 COMPLETED SERIES-BIASED 3-STAGE LNA

DESIGN FOR SYSTEMS USE

Conventionally, GaAs MMICs are biased with parallel drain supplies and additional negative gate voltage(s), requiring the sub-system designer to furnish a minimum of two supplies. By use of self-bias and an on-chip potential divider network, in conjunction with direct current recycling (or series bias), the benchmark amplifier described above has been modified to be

biased from a single supply (Figure 9). The supply is in the region of 12V with current drain equal to that of a single FET, thus reducing series regulation and self-bias losses. The completed chip is shown in Figure 10. Select-on-test bond pads are provided to program the operating current. During wafer test these can be grounded in turn to determine the correct operating point. The minimum area FET described above was used to create space for the additional decoupling capacitors and, as a result, the circuit also exhibits a gain slope, Figure 11, due to the reduced C_{gs}.

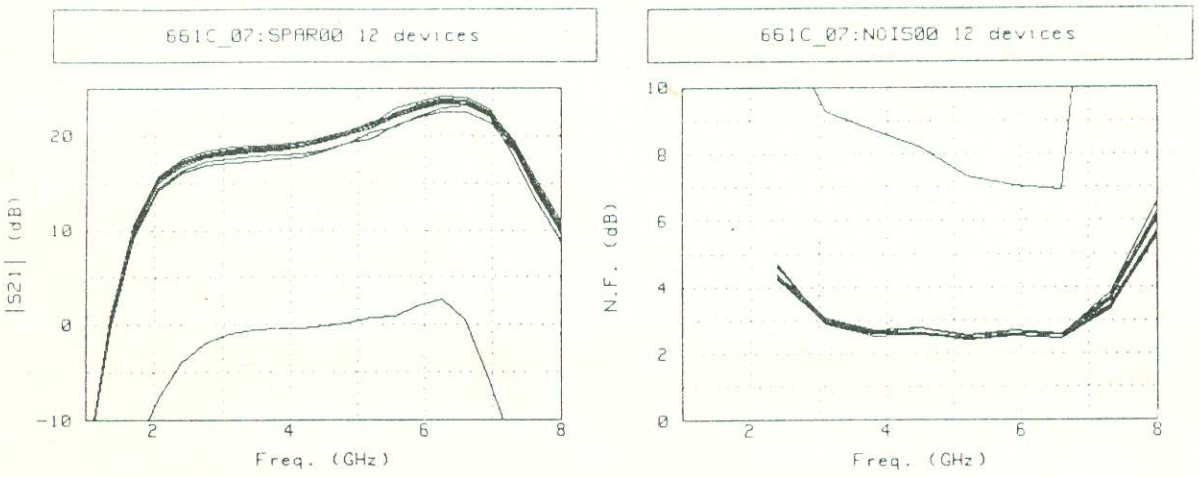


Figure 11 GAIN AND NOISE FIGURE OF SERIES-BIASED LNA, VD = 12V

The amplifier has been operated, with reduced gain, down to 8V/15mA compared with the original design which operated at 5V/75mA but also required a negative supply. This represents a DC power saving of over 60% for a gain reduction of approximately 3 dB.

CONCLUSIONS

The use of mid process RFOW has been conclusively shown to be a powerful technique. Top layer metal substitution has been shown by the examples given here not to be required for a high yield ion implanted foundry at C band. However, such a technique obviously will be appropriate when higher frequencies, an epitaxial process, or a HEMT foundry are considered.

The use of compressed topology techniques has been justified over five wafers, and some of the detailed techniques relevant to a specific foundry given. Series- and self-bias techniques have been applied to an amplifier to demonstrate direct and indirect DC power savings.

Examples of yield enhancement techniques have been given and their limits of applicability evaluated by the use of a demonstrator array, mid and post process RFOW, and the good process control available from a high yield ion-implanted Foundry.

ACKNOWLEDGEMENTS

The authors would like to thank A.J. Hughes, J.A. O'Kelly, G.T. Lloyd and the staff of the Plessey Foundry. This work was supported by RADC, US DoD, under contract No. F30602-87-C-0055. The help of John Rooks is acknowledged. This work was supported and sponsored in part by the Procurement Executive, Ministry of Defence (Royal Signals and Radar Establishment).