TECHNOLOGICAL AND GEOMETRICAL OPTIMISATION OF InP HBT DRIVER CIRCUIT

N. Kauffmann, S. Blayac, P. André, M. Riet, J.-L. Benchimol, A. Konczykowska
OPTO+, Groupement d'Intérêt Economique
France Telecom R&D
Route de Nozay, F-91461 Marcoussis Cedex
agnieszka.konczykowska@optoplus.fr

ABSTRACT

The design of high speed circuits and optimization in function of technological and geometrical parameters are presented. MUX-driver design and optimization for 40 Gb/s ETDM transmission illustrate the proposed approach. The impact of collector thickness (W_C) on driver performances is evaluated and assessed by circuit fabrication and measurements. 40 Gb/s electrical measurements of the realized MUX-driver module are presented.

INTRODUCTION

The important increase of communication services and particularly the data-transmission traffic needs to be supported by the development of adequate communication networks. High speed electronic circuits can be successfully used in high bitrate Time Division Multiplexing (TDM) transmission systems [1]. The constant progresses in semiconductor technology offer new possibilities to circuit designers. Single wavelength 40 Gb/s ETDM transmission has been demonstrated and could, in association with Dense Wavelength-Division Multiplexing (DWDM), allow to attain Terabit/s transmission rates.

TECHNOLOGY

An InP DHBT self-aligned technology has been developed at the OPTO+ laboratory [2]. This technology is well suited for the very high speed ICs and particularly for driver design because of good frequency performances (Ft and Fmax of 125 GHz and 83 GHz have been measured for Vce = 1.6 V and J = 0.8 mA/µm^2) combined with high gain (> 50) and high breakdown voltage (> 7 V). The use of a compositionally graded InGaAs base and self-alignment explains these good dynamic performances. In this technology both the transit time (graded base) and collector-base capacitance (collector undercutting allowed by self-alignment) are significantly reduced. Minimum emitter length and width of the transistors is 2.2 µm × 2.2 µm. Current densities up to 1 mA/µm^2 may be used without degrading the circuit reliability. The technology also provides three metallic levels, allowing optimisation of routing and layout symetrisation.

PREDICTIVE MODELLING

The successful design of high performance circuits must be supported by an important modelling effort. Rapid evolution and progress in semiconductor technologies require modelling which can answer both technology and CAD needs. In [3] we reported a realisation of the modelling tool ACPAR2A, allowing predictive design of high performance circuits using evolving HBT technology. The main function of ACPAR2A is to compute CAD models using analytical formulae in function of technological and geometric parameters. ACPAR2A has been used in a prediction-extraction scheme, serving in the first phase for device optimisation and lately for full-custom design (transistor sizing), once the technology is

validated and predicted model verified with parameter values extracted from measurements of realised transistors.

In the next section, we show how ACPAR2A can be used for evaluation of circuit performances in function of technological parameters.

MUX-DRIVER CIRCUIT OPTIMISATION

The MUX-driver circuit in the above-presented InP DHBT technology has been designed for 40 Gb/s ETDM system experiments with an Electro Absorption Modulator (EAM). The MUX-driver integrates two functions: last 2:1 multiplexing stage and EAM driver. Output swing above 2 V is one of the circuit specifications. The difficulty of this design lays in the combined requirements of a high bitrate and of an important output signal. One critical point in the design of the driver circuit is the choice of the optimal current density of the transistors. On one side, small transistors are required to satisfy high speed specifications, while an important current is necessary to obtain a high output swing.

Among different technological and process parameters, the collector epilayer thickness (W_C) is an important one because:

- W_C controls the important trade-off between the base-collector capacitance C_{BC} and the forward transit time τ_F
- W_C sets the high injection level and therefore the range of operating current of the transistor.
- W_C sets the breakdown voltage BV_{CE}

Besides, W_C can be easily set in the heterostructure epitaxial growth process. A more detailed analysis shows that a trade-off between two transistor parameters (collector transit time and capacitance) has to be set correctly to achieve best performances not only for the device but also for the circuit.

The transit time in function of Wc is presented in Fig. 1. In Fig. 2, the InP HBT transition frequency (Ft) is presented for 3 different Wc. The transistor emitter size is 19.2x2.2 μm^2 ensuring frequency and signal properties suitable for driver applications. The driver architecture was discussed previously [4] and following choices were made. The driver is composed of four stages, two differential current switches (CS) driven by emitter-followers (EFs) for level shifting and impedance transformation. For the third stage, three EFs have to be cascaded instead of the two used in E^2CL logic, because the impedance transformation is not very efficient at high frequencies. These EFs have to be carefully designed in order to avoid ringing, due to their inductive, low ohmic output, combined with their capacitive input. The layout must be carefully realised, and specially connections driven by EF stages.

In Fig. 3 and Fig. 4 we present two important aspects of the driver quality: output swing level and the time jitter. Simulations were realised in function of the driver speed and for different Wc values. It can be noticed that the optimal performance combining the necessary swing (>2 V) and limited time jitter can be obtained for the collector thickness Wc situated between 2500 Å and 3000 Å. In Fig. 5 eye-diagram simulations show the differences in the eye-opening and jitter for different Wc.

The circuit was fabricated with different layers standards (Wc = 1500, 2500, 3500 Å). Measurement results are in concordance with those predicted by simulation. Best results were obtained for Wc = 2500 Å. In Fig. 6, the measurement of the driver module (2.2 Vpp for 40 Gb/s) is presented. The circuit was realised and used in successful optical system experiments at 40 Gb/s transmission [4].

CONCLUSIONS AND PERSPECTIVES

In this paper we presented the MUX-driver optimisation in function of technological and geometrical parameters. It was shown that in addition to optimisation of planar geometrical parameters (transistor sizing) the influence of the layer structure can be evaluated and optimised for circuit applications. The performances of the MUX-driver for 40 Gb/s operation were simulated for different collector thickness. The predicted performances are in good agreement with the measurements of the realised circuit.

New perspectives for driver performances are opened by continuous technology progress (InP DHBT with 170 GHz F_T and 210 GHz F_{MAX} were reported in [5]).

This rapid technology progress assesses the need for tools, as those presented above, allowing to rapidly evaluate the impact of technological and geometric parameters on circuit performances.

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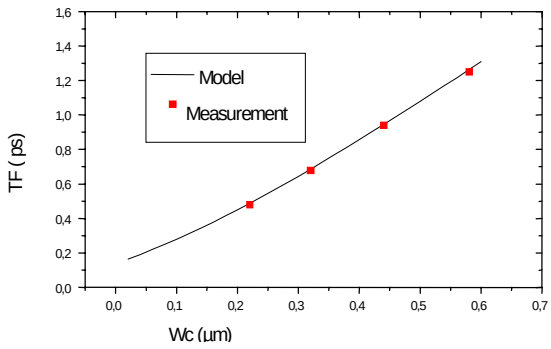

Fig. 1 Transit time in function of Wc

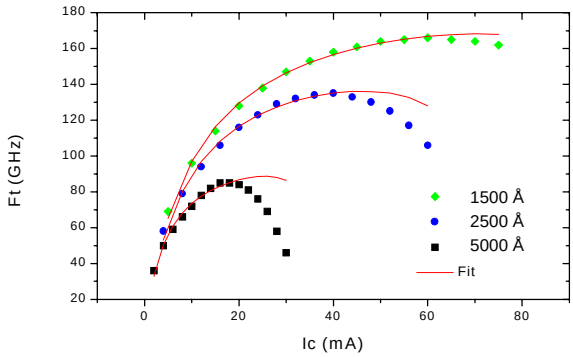

Fig. 2 Ft for different Wc

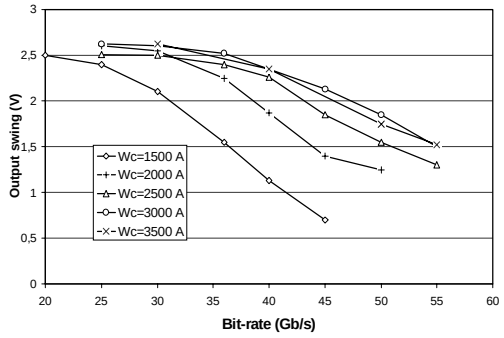

Fig. 3 MUX-driver output swing

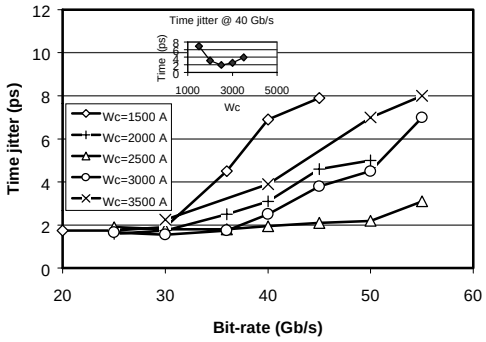

Fig. 4 MUX-driver time jitter

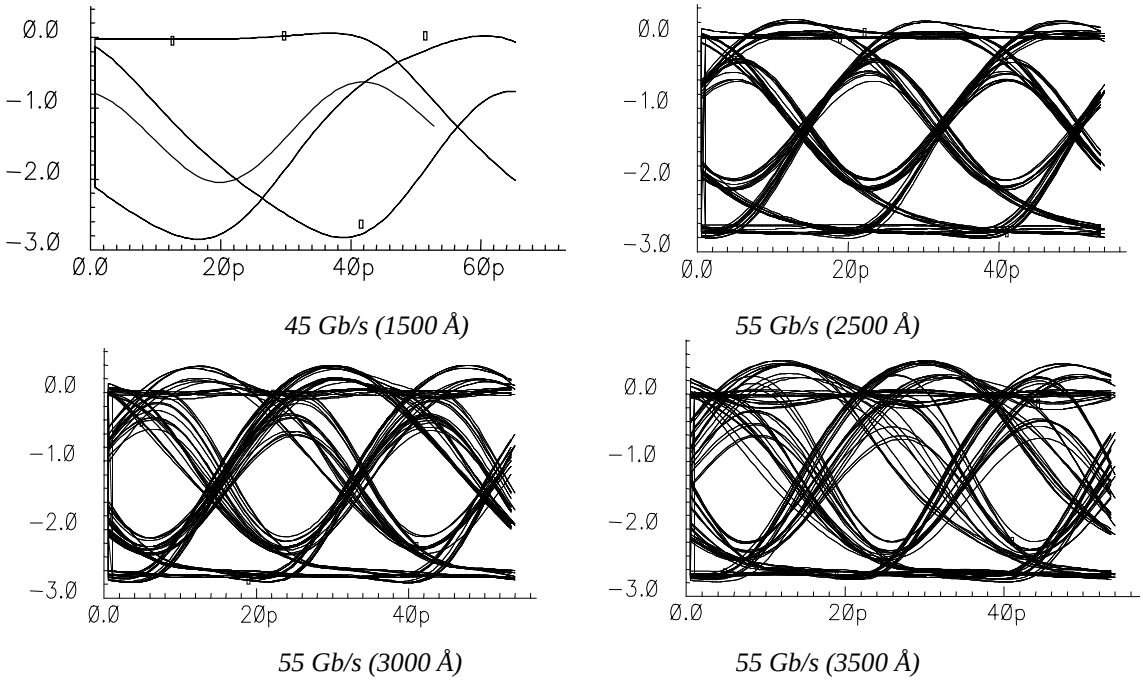

Fig. 5 Output signal simulation for different bitrates and different Wc

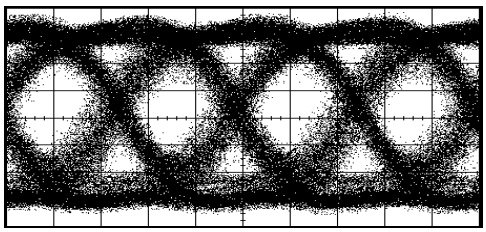

Fig. 6 MUX-Driver module measurement (40 Gb/s 2,2 Vpp)