TRANSISTOR SPECIFICATIONS AND SUBSTRATE DEFECTS IN GaAs TEST CIRCUITS

J.P. Fillard, M. Castagne, P. Gall, J. Bonnafe

ABSTRACT

It has been known for years that defects in GaAs wafers induce large perturbations and scattering in the specifications of transistors. Japanese workers (Y Nanishi) have performed extended investigations on this correlation using bidimensional mapping techniques whereas other people have used the so called Dense Row Pattern or matrix FET areas method. In this communication we present new results related to the inspection of microprecipitates revealed by Laser Scanning Tomography (LST). This high sensitivity technique allows us to obtain images of microprecipitates in the bulk material with especially high resolution and narrow sectioning specifications. It has been extended to the region underlying the surface just beneath the transistor channel. A statisticalevaluation of the threshold voltage and the side gating effect has been studied and correlated with the neighbouringmicroprecipitates.

INTRODUCTION

GaAs based integrated circuits are bound to give higher performances than those based on Silicon, nevertheless comparable scale integration has not yet been reached in spite of an unprecedented effort over the last 10 years. The reason for this failure mainly comes from the uncontrolled properties of the substrate in spite of a very impressive evolution in the quality of the standard material production [1].

The drawbacks preventing GaAs VLSI circuit fabrication are twofold first the large scattering of thespecification of individual transitors which limits the overall number of circuit elements and second, the "side gate " effect which limits the minimum distance between active circuits and electrical leads. These limitations have not hampered the reduction of the size of each transistor which achieves impressive standards: 0,25 µm technologies are available for years.

Investigations on GaAs bulk materials remains frustrating considering that the exact nature of the essential defect EL2 is still unknown. Also negative attempts to correctly has nevertheless become evident that FET performances are controlled by defects which must be located close enough to the channel or the inter electrode space in order toinduce a direct effect on the local electrical parameters.

The density of dislocations, impurity concentrations, EL2 and microprecipitates (MP) have been successively compared with the DC or HF or noise figures of FET test circuits arranged in a square matrix or linear arrays. The local situation is in fact quite complex and the correlation is not easy to establish.

Nevertheless the usual requirement [2] for a 1Kbit SRAM process (10^4 transistors) is to achieve V_{th} values with a standard deviation of under 15 mV for each wafer. Indium doping reportedly limits the disclocation density (EPD) and is known to give large improvements (though also with some drawbacks) ; high temperature annealing of the ingots is now considered a better solution. This definitely shows that the quality of the substrate influencesdramatically the homogeneity of the circuit fabrication.

In this paper we describe an investigation of the environment close to the channel of a series of implanted FETs on a LEC grown undoped Semi Insulating GaAs wafer. The exploration is made by high resolution Laser Scanning Tomography (LST) which effectively gives* a sensitive and precise image of the MPs in a very narrow region close to the transistor. The results and discussion aims at contributing to the present debate.

* Laser Scanning Tomography is not to be confused with simple ultramicroscopy experiment reported by Suchet and abusively called HRIT: this optical arrangement is very simple and convenient but in no way to be considered as tomographic neither high resolution.

Centre d'Electronique de Montpellier (LINCS Lab.). USTL - 34095 Montpellier Cedex 5

I - BACKGROUND:

A- Laser Scanning Tomography:

This technique was initially discovered by T. Ogawa [3] and further developped in Japan and in France [4,5,6,7,8]. Details of the experimental set-up can be found in references [3,7], the experiment (Fig -1) consists of an infra red laser beam which is focused onto a section of the wafer; a camera records the image of the bright scatterers illuminated along the path of the beam in the bulk material. The sample is moved forward by a step control and tsuccessive lines of the image are computer assembled to give a 2 dimensional view of a virtual plane parallel to the surface of the wafer.

This inspection method is perfectly non destructive and very sensitive because of the high illumination intensity and also the dark field conditions which allows a large gain for the video signal amplification. The usual limitation in optical microscopy of the short wavelengths does not apply as long as point source objects are involved. Scatterers in the nanometer range can be selectively detected up to densities in the range of $10^{13}cm^{-3}$.

LST has proved to be a very convenient tool to inspect semi conductor materials which reportedly are transparent in the near infra red region. Silicon, III-V compounds and Cadmium Telluride as well have been studied but GaAs is by far the most extensively refered to material [5,9,10].

LEC grown undoped materials typically show a structure of dislocations which are threaded into complex 3 dimensional bubble like "walls" defining a volume of defect free material ; the size of these cells usually lies between 100 and 700 μm in diameter. Comparison with images obtained by X ray transmission topography, surface etching, TEM etc...leads to the conclusion [7] that the LST image refers as well to MP arrangements. Individual particles are observed with varying size and likely chemical nature.

The largest MPs (0.1-0.2 μm) are known to be decoration precipitates located right on the grown-in dislocations [11]. Smaller MPs (10 nm) are clustered in the cell central zones in ingot annealed materials: some years ago Wacker empirically discovered that such annealings leads to large improvements in the electrical homogeneity of the wafers at the circuit scale. LST inspection gave the first evidence [8] that this was related to the central cloud of MPs which eventually comes from an evaporation/condensation process of the excess atoms from the decoration MPs during the temperature cycle.

From all our experience in this field it clearly appears that LST is able to reveal such defects in every materials. The sensitivity is so high that even in the free matrix of defect free In doped materials (Sumitomo) as well as top quality undoped annealed samples (Hitachi) there still exist numerous observable aggregates of reduced size.

In realty bulk materials and also epilayers contain large number of MPs, the role of which has been largely underestimated. A a rule of thumb for their observation is that : the smaller the particle the higher the density , observing such faint scatterers is not easy if they are imbedded in a cloud of bright scatterers but it becomes much easier in very good materials. It also occurs that when the density is too large the total image results in a foggy background but this is very typical and detectable. LST is an unrivaled method for inspection of submicron defects ; it can even be extended [12] to nanometer sectionning by computer assisted image analysis ; we called this technique Nanoscopy.

B- Role of the microprecipitates:

Large improvements have been introduced in the homogeneity of GaAs materials during recent years and as a consequence the scattering of the specifications of the transistors has conveniently decreased from 150mV to some 15 mV which makes it possible to fit within the LSI grade specifications. Even 8 mV deviations has been obtained on selected areas of improved VM FEC substrates[13]. Such high reproduciblity yield is of course exceptional and a contribution of the process fluctuations becomes of large importance in the result. The key parameter to checking the quality of the FETs is certainly the threshold voltage V_{th} (whatever the chosen definition of it may be).

Two different technologies can be used to make FETs on a semi-insulating substrate:

i) Epilayers : one would imagine that such grown structures would be independent of the defects in the substrate, especially if a buffer layer is placed between the transistor and the substrate. A longstanding question indeed has been to determine if the dislocations in the substrate are able to propagate into the layer during the growth process , the answer is not so clear but it is likely that the dislocation itself does not have so large influence on the electrical behaviour ; greaterer attention is to be paid to the decoration MPs located under the substrate surface ; these have recently been observed by O. Oda [14,15] on CVD layers and seen to directly perturb the pinch-off of the transistors to such an extent that the buffer layer is of no use. These particles contain large amounts of Arsenic which plays a role in the local epitaxy conditions. Furthermore, specific MPs located inside the epilayer were also reported by Oda after an AB etching investigation of thick layers (GaAs/GaAs); we have reached the same conclusion after a high contrast microscopy analysis on similar MOCVD structures [16]. These particles also reportedly cause problems in the carrier displacement on a microscale.

ii) Implanted layer : this is the most widely used technique for making "normally on" MESFETs on GaAs. Si^{29} is implanted at an energy of 50-150 KeV and for doses in the range of $10^{11}.10^{13} cm^{-2}$. This thickness of implantation is 1500-2000 Å and a final annealing is required to reconstruct the lattice damages.

Preliminary work by Hyuga [17], Kasahara [18] and Nanishi [19] have shown a correlation of FETs failure with the presence of a dislocation at a distance of shorter than 75 µm but it was not so clear what could be the physical relation. Macroscopic EPD has been observed to be correlated with V_{th} values which are also affected by the annealings and more locally by striations. A controversial proposition was given by Lee [20] and also Blakemore [21] relating the threshold fluctuation to the "walls" of the cell structure of LEC materials whereas Miyazawa [22] suggests the direct influence of the implanted atoms which introduces a high density of Si_{Ga} and Si_{As} defects close to the implanted zones.

Correlation a microsale has been was found by Ishii [23] for V_{th} and I_{DSS} with the cell pattern. Also the Carbon [24] was tentatively considered but its concentration in the walls has not been ascertained. Ingot annealings has proved to be effective for a better homogeneity and this procedure is known to produce uniform EL2 and impurities ; surprisingly a more detailed study [24,25] has revealed that the annealing operation does not improve the threshold of the worst FETs located in the walls but rather degrades the performances of the best FETs usually found in the cells.

The different patterns of test transistors previously used in these studies were :

i) a huge matrix ($20\text{-}30.10^4$ circuits) of automatically tested circuits. The total size is the wafer and the large number of data obviously requires computer assistance. This arrangement is very convenient for studying the large scale fluctuations (striations, fourfold EL2 distributions etc...) It is not at all adapted to local investigations of impurities or defects.

ii) the Dense Row Pattern (DRP)[26] is a linear array of 30 microFETs 300 µm long. This is very convenient to probe local profiles at a scale consistent with the cell dimensions ; it is unable to give long range information nor lateral behaviour.

iii) the microFET matrix [24] is a 6x8 matrix (350x500 µm2 of microFETs) which fits very well within local isotropic investigations of distributed perturbations.

From the above it can be deduced that dislocations, EL2, strain fields and impurities are all presumed to be indirectly concerned in the individual perturbations of the FETs. Our intent is to carefully evaluate the contribution of MPs to the behaviour of implanted FETs; we claim that such a study is only possible if we can arrive at exactly pin pointing the particles which lie in the immediate vicinity (micron range) of the circuit.

II - EXPERIMENTAL

A-Test circuits:

The wafer used is taken from a LEC grown standard GaAs unannealed 3" ingot which was checked by LST to display a usual cell structure of decorated dislocations. Test circuits of various configuration were prepared by Si^{29} implantation (150KeV energy and 3.10^{12} cm^{-2} dose). The recovery annealing is 20 minutes at 850°C.

Ohmic contacts are AuGeNi alloy for Source and Drain in a flat FET configuration. The surface of the wafer (outside the active zones) is passivated by Boron implantation and the leads are made using TiPtAu evaporations.

The test circuit is a double FET (200µm long): one has a large channel (50 µm) the other has a short channel (1 µm); each structure is provided with a side gating electrode located 50 µm from the channel. In this study only large FETs are investigated. It is to be kept in mind that usually such large channel FETs shows weakly perturbed V_{th}

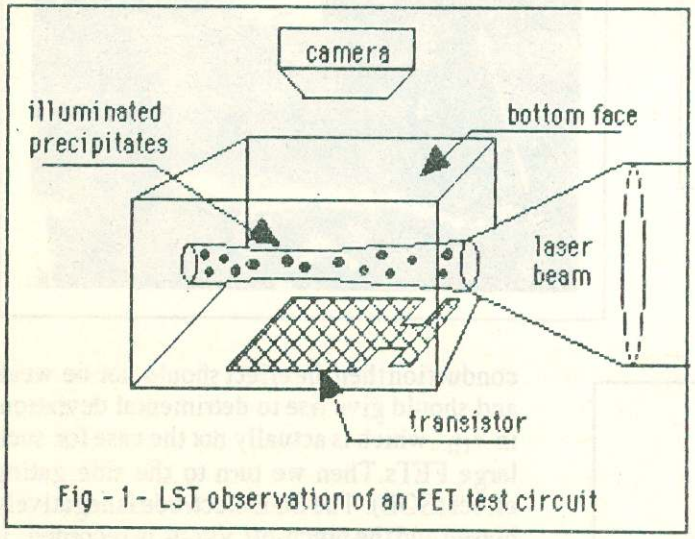

Fig - 1 - LST observation of an FET test circuit

; perturbations and scattering are of larger importance in shorter structures. On this wafer 50 circuits were analysed, the corresponding surface is a quarter of the wafer.

B - Electrical and LST measurements:

Electrical measurements are performed in the dark with a prober and usual DC checker. The standard conditions are V_{DS} = 5V and I_{DS} = 500 µA ; V_{th} is obtained at 10% I_{DSS} (at V_{GS}=0). The LST instrument has been described in many papers [see 3,4,5,9] ; the laser beam spot focus was improved to achieve a convenient spot reduction of less than 10 µm. A schematic view is given in Fig. 1. The circuit is placed upside down to make observation possible through the bottom face (previously polished).

III - RESULTS AND DISCUSSION

From the electrical analysis of 50 FETs it appears that the threshold voltage mean value $<V_{th}>$ and deviation σ_{th} are classical ($<V_{th}>$ = -2.152 V and σ_{th} = 0.0027 V). The spatial distribution of $<V_{th}>$ shows a long distance coherence in both the x and y directions (<110>) as evidenced in Fig -2 . This is to be related [28] to the long range variation of the electrical properties of the material (EL2°, EPD, Fermi level) . This is not surprising, considering that the size of the FET is comparable to the diameter of the "cells". Fig -3 shows an LST view of the defects in a region 10µm thick below a transistor. Dislocations, clouds of small MPs, isolated large MPs are the typical defect feature which can be selectively observed after adapting the illumination settings.

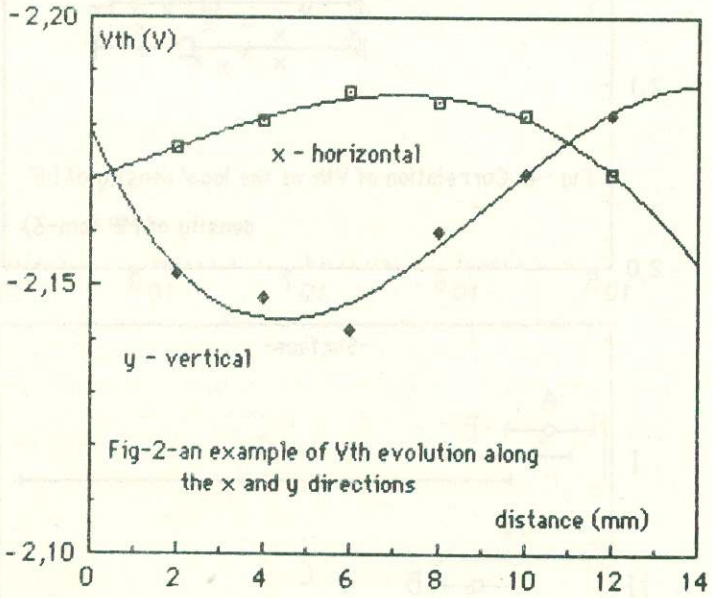

Fig-2-an example of Vth evolution along the x and y directions

The MPs are then observed and numbered for each transistor in a box of 10x100x200µm centered below the channel . Measurements are summarized in a graph (Fig -4) showing no special correlation between V_{th} and the density of MP (d_{MP}). For a better statistical insight the data is arranged in three classes (I is V_{th}<2.130 V ; II is 2.130 V< V_{th}<2.165 V and III is V_{th}>2.165 V); mean values and deviations are reported in Fig -4 (square dots); they do not reveal any noticeable difference. Nevertheless, in the present case the FETs are very large, thus averaging the Mp influence; further similar investigations will be performed on shorter structures. It can be imagined that if MPs play a role in the channel

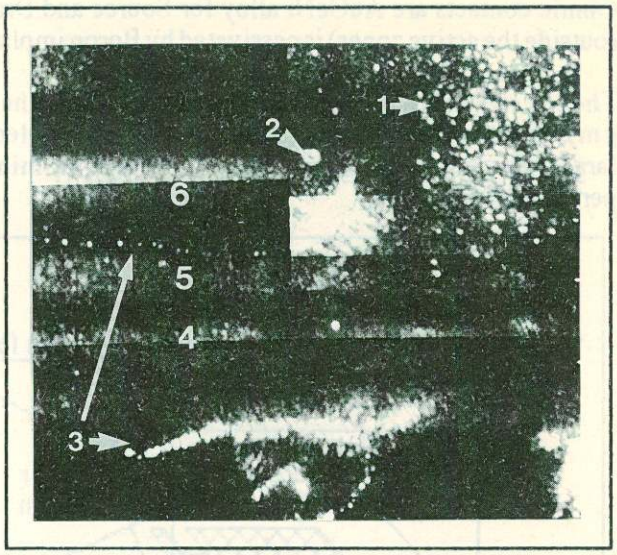

Fig -3 : LST view of the 10µm region below an FET
1- cloud of small MPs revealed at high illumination level
2- isolated big MP
3- decorated dislocations
4-Source ohmic contact
5- Drain ohmic contact
6- Side gate Ohmic contact

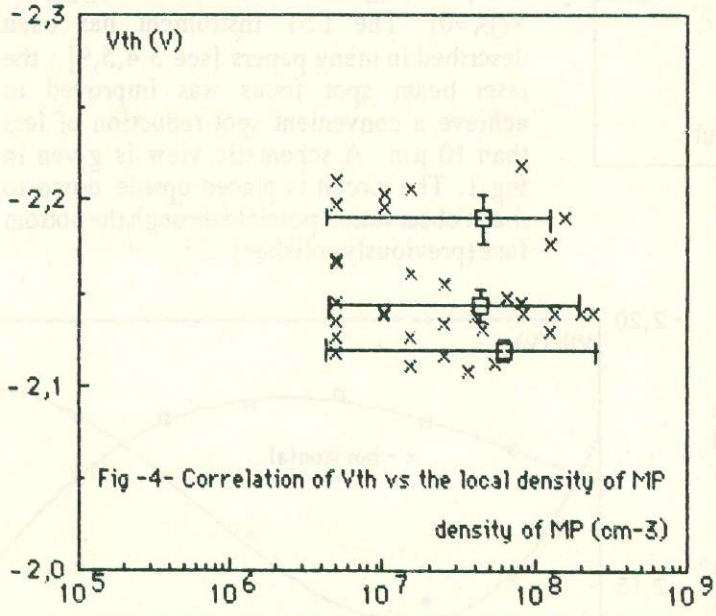

Fig -4- Correlation of Vth vs the local density of MP

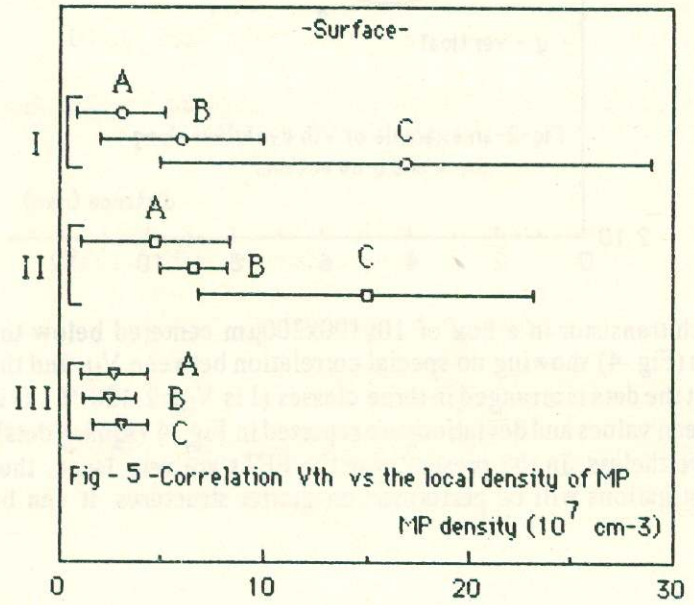

Fig - 5 -Correlation Vth vs the local density of MP

conduction then the effect should not be weak and should give rise to detrimental deviations in V_{th}, which is actually not the case for such large FETs. Then we turn to the side gating effect (SGE). The SGE electrode is negatively biased and the pinch-off V_{SGE} is recorded. It soon appears that there are very large variations of V_{SGE} and circuits are filed into three categories: A- for $V_{SGE} < -20$ V; B- for $-20\ V < V_{SGE} < -14$ V ; C- for $V_{SGE} > -14$ V. Obviously A category refer to "good" circuits and C to bad ones. Again no direct relation is observed between V_{SGE} and V_{th} and the two parameters are certainly not influenced by the same defects. We then we obtained LST information on the MPs in the interelectrode sublying volume. Three layers are explored and refered to as I, II, III : I is a 10x100x200 µm box between the SG electrode and the Drain. II is a 20µm thick similar box and III is a larger box 30x260x350µm which includes all the volume under the total circuit (FET and SG electrode).

The density d_{MP} is in the range of 10^7-10^8 cm^{-3} in good agreement with Oda's observations [1,3] after AB etching micrography. The data are resumed in the Fig -5 for the three boxes (I,II,III) and the three classes of V_{SGE} (A,B,C). It clearly appear that:

i) in the 10µm layer (I) the more the MPs the worse the side gating: the mean values and deviations are separated.

ii) in the 20µm layer (II) the difference is reduced

iii) in the 30µm layer the statistical discrimination is removed and V_{SGE} is indifferent to d_{MP}.

It can be confidently concluded that the MPs located in a 10 µm layer below the surface in the interelectrode volume are the only precipitates which can control the side gating effect; there is an active zone which causes the leakage current flow; deeper defects in the bulk have a negligible effect.

The side gate drawback could thus be counteracted very simply by a deep recess surrounding the transistor , as suggested by Blanpain [27]. Unfortunately such structures would be very cumbersome in an LSI process. It should be preferable to directly reduce the density of MP at the surface of the wafer by consistent annealings.

CONCLUSION

From this work on large FETs it can be concluded that MPs are not able to drastically influence the behaviour of the channel conduction whereas they are directly involved in the SGE perturbation. The volume to consider for SGE is limited to a layer 10 µm thick between the SG electrode and the Drain.

ACKNOWLEDGEMENTS:
Authors are indebted to Dr M Bonnet and Pinsard (Thomson TCM) for providing test circuits and for helpful discussions. This work was supported by DRET and CNET contracts.

REFERENCES

[1] J.P. Fillard - Ann. Telecomun. 42, 3-4, 149 (1987)
[2] G. Nagel, M. Baumgartuer, K. Lôhnert, P. Deconinck, P. Suchet, J.P. Farges, G.M. Martin - Vth Annual Esprit Conf. Bruxelles (1988)
[3] K. Moriya, T. Ogawa - Japn. Jour. Appl. Phys. 22 L207 (1983)
[4] P. Gall, J.P. Fillard, M. Castagne, J.L. Weyher J. Bonnafé - Jour. Appl. Phys. 64 5161 (1988)
[5] J.P. Fillard, P.C. Montgomery, P. Gall, M. Castagné, J. Bonnafé - DRIP III Tokyo (Sept. 1989) Proc.to appear Jour Cryst Growth.
[6] J.P. Fillard, P. Gall, M. Castagné, J. Bonnafé - "Gettering and defect engineering in Semi-Cond. Technology", Berlin (Oct. 1989) Sci. Tech. Pub. LD. M Kittler Ed.
[7] J.P. Fillard - SPIE Conf. (Cannes) 866 10 (1987).
[8] T. Ogawa, N. Nango - Rev. Sci. Inst. 57 1135 (1986)
[9] T. Katsumata, H. Okada, T. Kikuta, T. Fukuda - Appl. Phys. A 42 103 (1987)
[10] P. Gall, J.P. Fillard, J. Bonnafé, M. Castagné, J. Weyher, A. George - DRIP II Symposium E. Weber Ed. 44 215 Elsevier (1987)
[11] P.C. Montgomery, J.P. Fillard, Mes. Sci. Technology 1 (1990)
[12] JP Fillard, PC Montgomery, P Gall, J Bonnafé, M Castagné - DRIP III Tokyo (Sept. 1989) Proc.to appear Jour Cryst Growth.
[13] P. Suchet, M. Duseaux, J. Maluenda, G. M. Martin - Jour. Appl. Phys. 62 1097 (1987)
[14] H. Yamamoto, O. Oda, M. Seiwa, M. Taniguchi, H. Nakata, M. Ejima , J. Elec.Chem. Soc., 136 10 (1989).
[15] H. Yamamoto, H. Shimakura, G. Kano, M. Seiwa, H. Nakata, O. Oda - Proceedings of the Int. Conf. Sci. Tech. of Defect Control in Semiconductors (1989).
[16] P.C. Montgomery - unpublished results
[17] F. Hyuga - Japn. Jour. Appl. Phys. 24 L160 (1985)
[18] J. Kasahara, M. Arai, N. Watanabe - Elect. Lett. 21 1040 (1985)
[19] Y. Nanishi, S. Miyazawa, Y. Matsuoka - DRIP I Symposium J.P. Fillard Ed. Elsevier 31 225 (1985)
[21] P. Dobrilla, J.S. Blakemore - DRIP I Symposium J.P. Fillard Ed. 31 Elsevier 127 (1985)
[20] R.E. Lee, A.T. Hunter, R.P. Bryan, H.M. Olsen, H.W. Winston, R.S. Beaubien - GaAs-IC Symposium Boston (1984)
[22] S. Miyagawa, Y. Ishii, S. Ishida, Y. Nanishi - Appl. Phys. Lett. 43 853 (1983)
[23] Y. Ishii, S. Miyazawa, S. Ishida - IEEE Elec. Dev. 31, 1051 (1984)
[24] M. Van Hove, W. de Raedt, M. de Potter, J. Van Rossum, J.L. Weyher - MRS Fall meeting Boston (1987)
[25] S. Miyazawa, K. Watanabe, J. Osaka, K. Ikuta - Rev. Phys. Appl. 23 727 (1988)
[26] J. Maluenda, G.M. Martin, H. Shink, G. Packeiser - Appl. Phys. Lett. 48 715 (1986)
[27] E. Blanpain, T. Kamiya, Jap. Phys. Soc. Meeting ED 85-107 (1985)