HIGH PERFORMANCE GaAs MONOLITHIC TRANSIMPEDANCE AMPLIFIERS FOR MULTIGIGABIT PER SECOND FIBER OPTIC LINKS

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ABSTRACT

A new design approach for MMIC transimpedance amplifiers is described, which allows substantial improvements as noise, gain and stability over the previously reported circuit solutions. An accordingly designed MMIC transimpedance amplifier we constructed and tested is described.

1. INTRODUCTION

As well known fiber optic presents great advantages over conventional transmission means, in terms of bandwidth, attenuation, electromagnetic coupling immunity, size and cost.
The state of the art repeaters (signal regeneration circuits) of fiber optic links are based on an electronic signal treatment because the basic technology for direct optical processing is not yet sufficiently developed and reliable for network implementation. For this reasons, opto-electronic and electro-optical conversions are needed, the first one being usually achieved through PIN or APD diodes, the second through laser diodes. An important repeater portion, usually called front-end, is constituted by the photodiode and the preamplifier, where the diode photocurrent is injected. This circuit practically determines the repeater noise performance, or in the other words, the link bit error rate (BER).
The preamplifier bandwidth (expressed in cicles/sec), must be nearly equal to the bit rate (in bit/sec), because the reduction of intersymbol interference requires the use of a rised cosine type equalizer. The amplifier can be constructed both in hybrid or in MMIC form. The last one is preferable for reproducibility, reliability, and cost reasons, and requires d.c. coupled designs for the difficulty of constructing the high value capacitors needed for achieving the required low frequency cutoffs in the KHz range. Two basic approaches are available for the amplifier design: transimpedance or classical amplifier-equalizer [1, 2]. The first solution is largely preferable in high bit rate systems for the wider bandwidths allowed [1] and for the difficult design of the equalizer section in the second solution.
In this paper we describe the major achievements of an organic and systematic work, which starting from our system requirements and from a critical knowledge of the more advanced research results in the field, has lead, through the study of various monolithic prototypes, to the design and the construction of a MMIC transimpedance amplifier (for 2.5 Gb/s fiber optic links) with extremely advanced performances. So, by using the results of in house developed d.c. [3] and small signal models, we will first study the front end noise performance with the aim of establishing significant guide lines for its design.
Subsequently, the transimpedance amplifier (TIA) performances achievable with well known GaAs MMIC amplifier topologies [4, 5] will be discussed. Then, the design of a cascode type [5] monolithic amplifier we developed will be described and its measured performances critically analyzed. Having so demonstrated the substantial unadequacy (unless as for our system front-end specifications) of the known TIA circuit approaches, a new amplifier topology will be described allowing substantial performance improvements, in terms of noise, bandwidth, TIA gain flatness and circuit stability. Finally the design and the performances of a monolithic TIA having the new circuit topology will be reported.

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2. FRONT-END NOISE ANALYSIS

In this paragraph we report a front-end noise analysis whose results will constitute the basis of subsequently developed design considerations.
It is supposed that a typical commercially available InGaAs avalanche photodiode (APD) is employed (Fujitsu FPD13U51SR) and that the bandwidth of the MMIC preamplifier to be designed is equal to the system bit rate. Moreover, it is assumed that all the devices are produced with the Telettra standard A process (1 um gate length, 3 volt pinchoff). Typical parameters for a 100 um wide device, obtained with this process, are given in table (1).
Our fiber optic system requires that a minimum mean optical power level of -35 dBm be feed to the APD. Using a non return zero (NRZ) transmission code and requiring a BER $\leq$ 10e-9, the front-end signal to noise ratio must be $\geq$ 16 dB [6]. Such a ratio can be easily evaluated by making reference to TIA input noise current [1, 2], which is given by the quadratic sum of different contributes such as: APD current, feedback resistor noise and equivalent gate noise of the first TIA MESFET device. Such contributions can be calculated as follows.
APD noise current ($\langle Iapd^2 \rangle$). It is given by the shot noise PN junction relationship [7] with some typical values for 50 um diameter InGaAs diode:

$$\langle Iapd^2 \rangle = 2q * [Ids + (Idb + Is) * M^{(2+X)}] * I2 * B \qquad (1)$$

where: q=electron-charge (1.6e-19C); Ids=dark superficial current (10 nA); Idb=dark built-in current (5 nA); M=average gain multiplication factor (typically ranging between 10 and 12 as a required to trade-off between optical dinamic range and bandwidth) X=excess noise factor (0.7); B=operating bit rate (2.5 Gb/s); Is=mean primary photocurrent (Responsivity * mean optical power); I2=weighting function (W.F.) [2], dependent only on the shapes of the input optical pulse and of the equalized output pulse (for NRZ coding and equalized output pulse with full raised cosine spectrum, I2=0.56).
Feedback resistor noise current ($\langle IRF^2 \rangle$). This contribution, is given by the well known relationship:

$$\langle Irf^2 \rangle = 4KT * I2 * B/RF \qquad (2)$$

where: RF=feedback resistor; I2=W.F. (0.56); B=bit rate; K=Boltzmann costant; T=absolute temperature.
Equivalent gate noise current of the first TIA MESFET device ($\langle Ieq^2 \rangle$).
For a FET device working in the minimum noise conditions (Ids $\simeq$ 0.25 Idss) [8], taking into account thermal, 1/f, active load and gate induced noise contributions [2], the equivalent TIA noise current can be written as:

$$\langle Ieq^2 \rangle = 4KT * P * (2*6.28*Ct)^2 * (1/gm) * [fk*If*B^2 + I3*B^3] \qquad (3)$$

P=technology and bias dependent factor (3.5); If=W.F. (0.184); I3=W.F.[2] (0.0868), gm=MESFET transconductance; B=bit rate (2.5 Gb/s); Ct=Capd+Cgs; Cgs=MESFET gate to source capacitance; fk=1/f corner noise frequency (10 MHz).
The Ct^2/gm value, proportional to $(Capd+Cgs)^2/gm$, is minimized for Cgs = Capd. Thus, from the knowledge of the gate to source capacitance per unit gate width at Ids = 0.25 * Idss (tab. 1), it is easy to deduce the first FET gate width (Wg): since Capd = 0.5 pF, we obtain Wg = 450 um, gm = 31 ms. From equation (2) it follows that another parameter for minimizing the overall TIA input noise current is the value of the feedback resistance RF, which (see equation 2) must be sufficiently high to guarantee a front-end S/N $\geq$ 16 dB. The minimum RF value is here determined with the aid of two plots shown in fig. 1. The first one, is deduced from the relationship:

$$S/N = 16\ dB = 39.8 = [(\langle Is \rangle * \langle M \rangle)^2] / [\langle Iapd^2 \rangle + \langle Itia^2 \rangle]$$

where:$\langle Itia^2\rangle=\langle Irt^2\rangle+\langle Ieq^2\rangle$. It gives $\langle Itia^2\rangle$ as a function of the optical repeater input power for different mean values of the APD multiplication factor <M>. The second diagram, gives $\langle Itia^2\rangle$ as a function of the feedback resistance RF. Fig. 1 shows that an optical power level of -35 dBm can be reached if RF $\geq$ 1000. Moreover the use of high feedback resistors allows higher preamplifier gain to be obtained, thus resulting both in a lower next stage noise contribution, and in a reduced necessity of other amplifier stages.

3. CRITICAL ANALYSIS OF THE AVAILABLE TIA SOLUTIONS

In order to simplify the analysis and the result comparisons, it is assumed that the circuits studied in this section are loaded with an infinite output impedance. This assumption is not restrictive because the output matching to a desired load impedance (i.e. 50 ohm) can be easily achieved, with small bandwidth loss, using a source follower output stage, which imply about 6 dB gain reduction.
The simplest TIA topology is shown in fig. 2 and is obtained by applying a shunt resistive feedback around a single common source inverter [4]. Active loads are usually preferred for monolithic circuit implementation, in spite of some noise performance degradation, because of the inherent high gain, d.c. power saving and insensitivity to process variations. For the fig. 2 circuit, the following transimpedance (Ht) and voltage gain (Gv) relationships are hold true:

$$Ht(jw) \simeq Rf / (1 + jwCtRf/Gv) \qquad (4)$$

$$Gv = Vout/Vin \simeq gm1/(gd1+gd2) \simeq 4gm1/5gd1 \qquad (5)$$

where w is the angular frequency, gm1 and gd1 the transconductance and output conductance of the FET1, gd2 the output conductance of the FET2. Using the table 1 results one obtain from (5) Gv = 15.5 dB, from (4) and RF = 1 Kohm, transimpedance cutoff frequency fc = 955 MHz.
This is insufficient for our bandwidth requirements (2.5 GHz). In order to obtain this bandwidth, for a single pole transimpedance transfer function a voltage gain of 24 dB is needed. Thus an increase of the feedback stage gain is required.
This could be, in principle, done by applying the resistive feedback to a cascade of three inverters but this solution is not recommendable for broadband circuits. In fact the signal phase shift increase with frequency, leads to working conditions where the feedback becomes regenerative. More adequate appears the inverter-noninverter combination allowed by the recently proposed [5] cascode topology, shown in fig. 3. This circuit was computer optimized for maximum gain voltage and the devices parameters listed in fig. 3 were obtained. For a correct application of the scaling rules, a minimum FET width limit of 50 um was set in the optimization [9]. Curve a in fig. 4 gives the optimized voltage gain vs. frequency, when the shunt feedback FET is removed: a gain cutoff frequency of 1.4 GHz is observed. Because the gain is much higher than the value needed for using feedback resistor of $\geq$ 1 Kohm, the feedback shunt FET depicted in fig. 3 was used for achieving broader bandwidths. A gain-bandwidth optimization yielded the results of fig. 4 curve b, where a cutoff frequency of 2.8 GHz is shown. The circuit was constructed in MMIC form [3] and a voltage gain nearly equal to the one of fig. 4 curve b was deduced from S parameter measurements. The measured transimpedance amplifier gain with an input connected 0.5 pF APD capacitance and with 50 ohm load is shown in fig. 5, when a relatively unsatisfactory transfer function peaking is evident. This peaking was ascribed to the parasitic capacitances vs. ground in the feedback loop leading to a relatively low stability phase margin. In fact potential instability regions ($|S11|>0$) usually produce sharp peakings in the transimpedance function, which as well known, is proportional to $|S21| / (|1-S11|)$. To correct this situation we inserted, as suggested in [5] an R-C parallel network between ground and the feedback FET source. Optimization under such conditions showed the substantial unadequacy of this system to obtain considerable improvements in the stability phase margin.

4. THE NEW TIA CIRCUIT TOPOLOGY

The above described MMIC circuit suffers from two drawbacks: a stability phase margin too low and the need of a non-standard bias voltage. In order to solve the first problem we decided of reducing the signal phase delay along the feedback loop, by introducing a compensating zero in the amplifier voltage gain. This was obtained by applying the well known concept of the "feed forword compensation" [10] where a reduction of the phase shift is obtained, for a simple vector summing rule, by renjecting the input signal after the first amplifier portion. The resulting TIA amplifier topology is shown in fig. 6.
Here we see that a decoupling buffer is inserter between the common source inverter and the grounded gate non inverting circuit. The buffer permits the d.c. voltage level shift necessary for reintroducing the input signal into the gate of the non inverting device and decouples the drain of the inverting device from the source of non inverting one. This allows the use of standard $\pm$ 5 volt bias supply and results in a little amplifier voltage gain increase.
This situation is shown in fig. 7 where the voltage gain of three circuits is reported. In fig. 8 the transimpedance calculated for the some circuits of fig. 7 is reported vs frequency. The new topology results in a flatter transfer function; moreover its better stability performances are proven by the fig. 9 reflection coefficient data with the complete desappearing of the potential instability ($|S11|>1$) region.
The TIA having the feed forward topology was constructed in monolithic form (see fig. 10 for the 1.2 x 1.2 mm^2 circuit photograph). The chip power consumption was 900 mW, its measured equivalent input noise at 1 GHz is 6 pA/V $\sqrt{HZ}$. A detailed description of the amplifier experimental results will be given in the oral presentation.
Monolithic TIA having the FF topology and better performances are now under development using 0.5 um gate length devices and an "ad hoc" developed low power consumption technology. Here, in order to reduce the single device power consumption, for a fixed transconductance value, the saturation current Idss was minimized. To this end the active devices of the monolithic chip was fabricated on Si29 properly implanted active layers: the implantation energy was 100 Kev and the dose 3.5e-12 cm-2. A slightly recessed (300 Å) channel was fabricated thus producing FET Idss of 100 mA/mm. Moreover the MESFET device "knee" was reduced by lowering the source resistance through the use of N+ selectively implanted areas and the decrease of the gate to source distance.

5. CONCLUSIONS

The major achievements have been described on an organic work, which starting from our system requirement for 2.5 Gb/s fiber optic link, has lead to the design and construction of MMIC amplifiers with extremely low noise, gain bandwidth and stability performance. A new cascode feed forward type circuit topology of basic importance in achieving such results has been described in detail.

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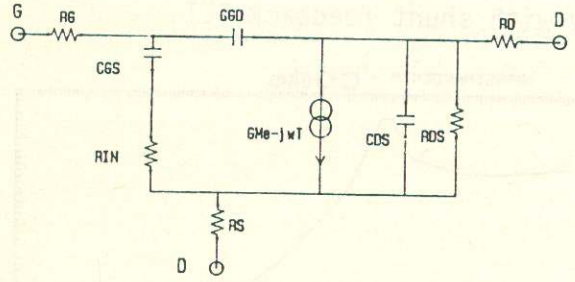
TAB I

TELETTRA A PROCESS (Idss/mm=250mA Vp=3volts Lg=1um ft=10GHz) small signal equivalent circit



Wg=100um Idss=25mA	Wg=100um Ids=12mA	Wg=100um Ids=6mA
Vgs=0 Vds=2.5	Vgs=-1.5 Vds=2.5	VGS=-2 Vds=2
RG=2 RS=6 RD=15 RIN=9 CGS=0.15pF CGD=0.007pF CDS=0.02pF GM=11mS RDS=1500 TAU=5ps	RG=2 RS=6 RD=15 RIN=12 CGS=0.13pF CGD=0.0076pF CDS=0.02pF GM=10mS RDS=1000 TAU=5ps	RG=2 RS=6 RD=15 RIN=18 CGS=0.11pF CGD=0.007pF CDS=0.02pF GM=8mS RDS=1200 TAU=5ps

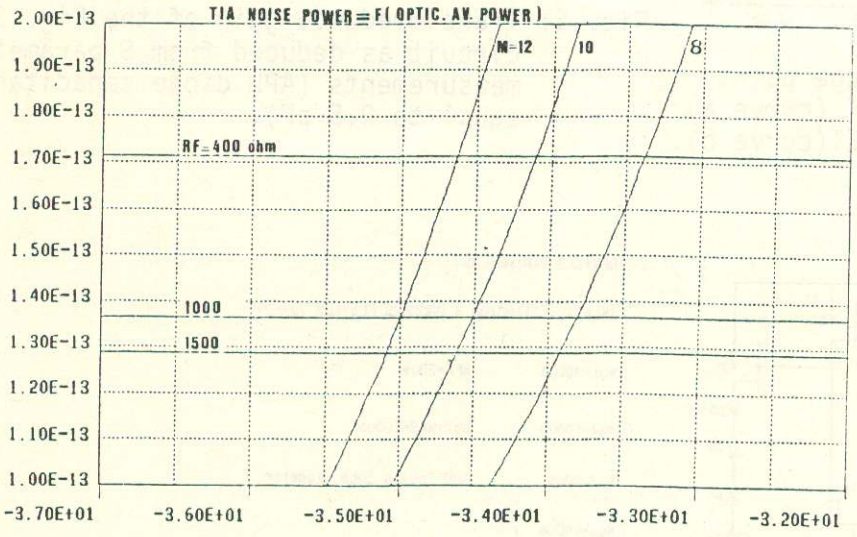


Fig. 1 : Vertical curves: TIA equivalent input noise current $< I^2tia >$ *vs.* optical mean power for various $< M >$, calculated for a BER = 10^{-9}. Horizontal curves: $< I^2tia >$ for different RF values.

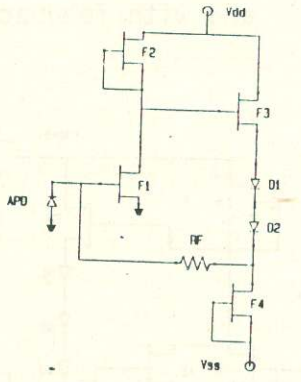


Fig. 2: Single inverter source follower TIA topology.

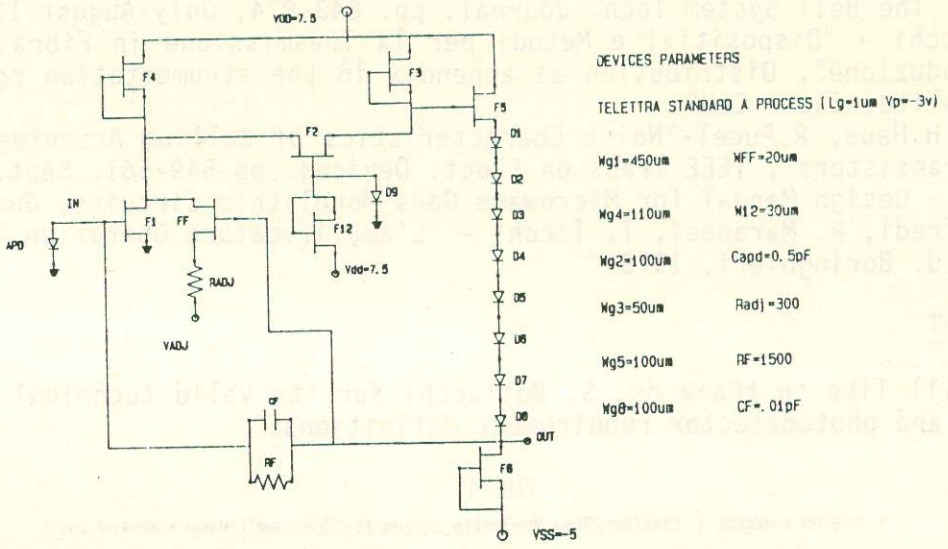


Fig. 3 : Cascode TIA topology with shunt feedback FET.

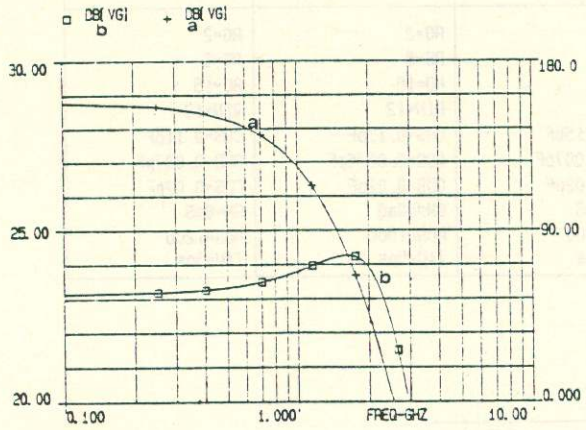


Fig. 4: Fig. 3 circuit voltage gain: with no feedback FET (curve a) and with feedback FET(curve b).

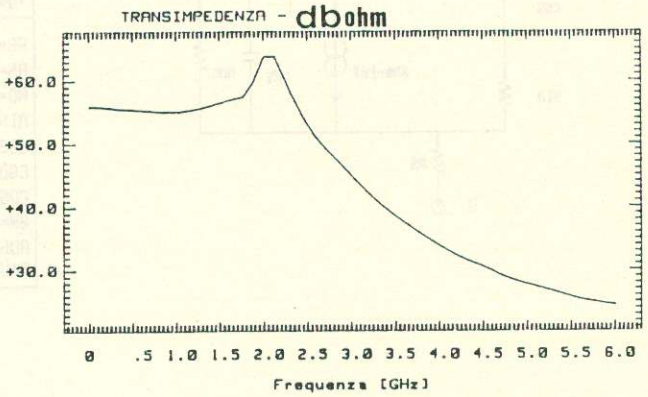
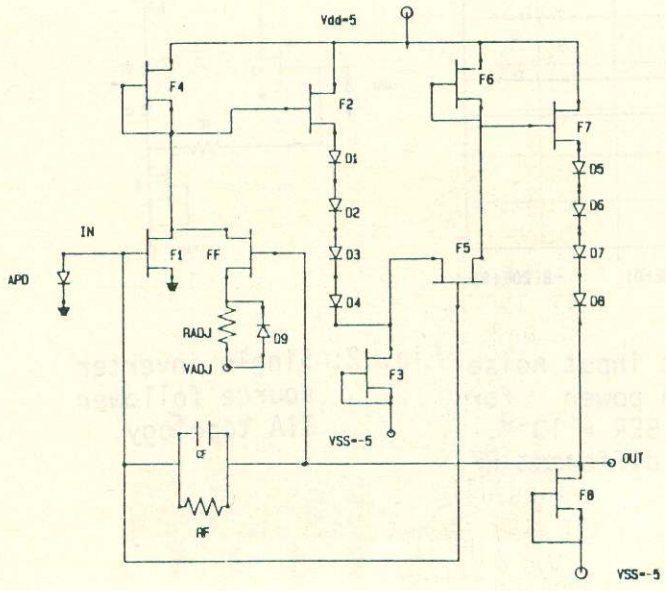


Fig. 5: Transimpedance gain of the Fig. 3 circuit as deduced from S parameter measurements (APD diode capacitance equal to 0.5 pF).



DEVICES PARAMETERS

TELETTRA STANDARD A PROCESS (Lg=1um Vp=-3v)

Wg1=400um WFF=20um

Wg4=100um Wg7=Wg8=100um

Wg2=80um APD InGaAs 50um diameter

Wg3=100um

Wg5=100um

Wg6=50um

Capd=0.5pF

Radj=600

RF=1500

CF=.01pF

Fig. 6 : Feed forward (FF) TIA topology.

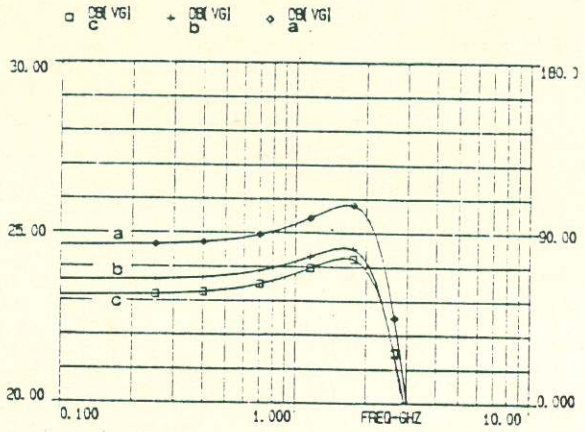


Fig. 7 : TIA voltage gain vs. frequency for different circuits: gain-bandwidth optimized FF topology (curve a), same topology with no signal reintroduction (curve b), cascode circuit with no decoupling buffer (curve c).

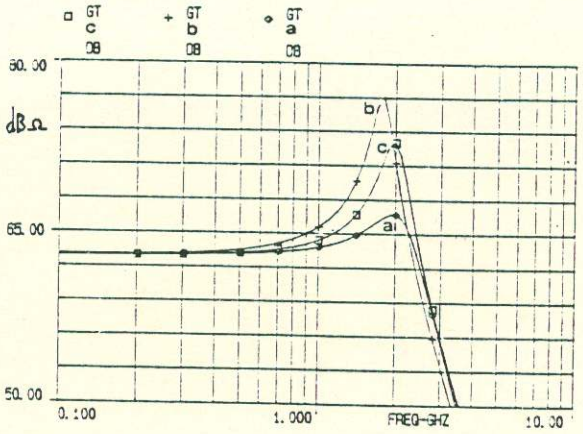


Fig. 8 : Transimpedance gain vs. frequency for 0.5 pF APD capacitance for the same circuits of Fig. 7.

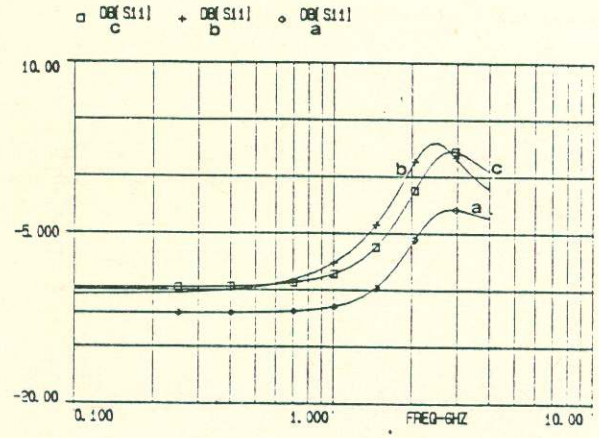


Fig. 9 : Input reflection coefficients vs. frequency for the Fig. 7 circuits.

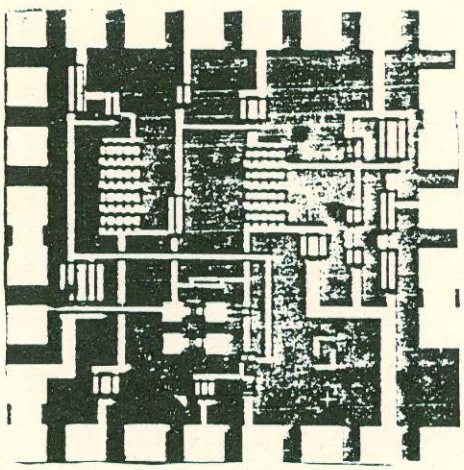


Fig. 10 : Photopgraph of the 1.2x1.2 mm^2 MMIC chip having the FF new topology.