

Small signal and power performance of AlGaIn/GaN HFETs grown on s.i. SiC

A. Wieszt, R. Dietrich, J.-S. Lee, A. Vescan, H. Leier, E.L. Piner^a, J.M. Redwing^b

H. Sledzik^c

DaimlerChrysler AG, Research and Technology, P.O. Box 2360, D-89013 Ulm, Germany
phone:+49-731-505-2087 / fax: +49-731-505-4102 / email: andreas.wieszt@daimlerchrysler.com

^aATMI/Epitronics, 21002 N. 19th Ave., Phoenix, AZ 85027, USA

^bPenn State University, Dept. Of Materials Science and Engineering, University Park, PA 16802, USA

^cDaimlerChrysler Aerospace, Woerthstrasse 85, D-89077 Ulm, Germany

ABSTRACT

We report on the DC, the small signal and the RF power performance of AlGaIn/GaN HFETs grown on semi insulating (s.i.) SiC substrate. DC characterization shows a record transconductance of 300mS/mm for a device with a gate length of 0.3 μ m. Load pull measurements at 10 GHz were performed, indicating output power levels above 4Watts cw for a unpassivated 1.6mm device. Finally, standard equivalent circuit parameters are extracted and verified for devices with different gate widths.

INTRODUCTION

The high operating voltages, the high breakdown voltage, the saturation velocity of electrons in AlGaIn/GaN heterostructures and the excellent thermal conductivity of SiC as a substrate material makes GaN on SiC the right choice for future power amplifier and switching devices in a variety of military and commercial wireless communications applications. For example, Wu et.al. (1) demonstrated power densities at X-band, which are several times higher than GaAs based FETs. This correlates quite well with the theoretical predicted power densities of Weitzel (2) for AlGaIn/GaN power FETs on SiC.

To develop a model of an high power amplifier, it's necessary to perform DC-, pulsed-, small signal-, and large signal-characterization of the FETs, from which the data to be used in an amplifier design is extracted.

TECHNOLOGY

The devices used for the characterization, were fabricated on epitaxial GaN layers, which were grown on s.i. SiC in a horizontal MOCVD reactor at 1100°C. A 100nm AlN nucleation layer, a 2 μ m GaN buffer and a top AlGaIn barrier/supply layer were deposited on the SiC. The AlGaIn structure consists of a 3nm undoped spacer, a 10nm Si-doped ($1 \times 10^{19} \text{cm}^{-3}$) supply and a 5nm undoped cap layer. The Al-content is 25%.

Device separation was performed by RIE in a BCl₃/Ar- atmosphere. Ohmic contacts were fabricated using a Ti/Al metallization annealed in a N₂ ambient at 900°C for 30s. The contact resistance was characterized by TLM method. The measured values are between 0.3 and 0.5 Ω mm. The 0.3 μ m T-shaped Ni gate was defined by e-beam lithography. For large periphery devices, up to a gate width of 1.6mm, multi-finger structures with 3 μ m Au airbridges were used.

DC, RF AND LOAD PULL MEASUREMENTS

After processing, the devices were analyzed by DC, RF and power measurements. The DC measurements showed for 2x50 μ m devices a maximum drain current (at V_{gs}=+1V) of 1.5A/mm and a maximum transconductance of 300mS/mm at V_{ds}=10V, which is one of the highest ever reported for this gate length ([figure 1](#)). At higher V_{ds} the output current and the transconductance are reduced due to self heating of the device. The self-heating becomes also significant as the periphery of the FETs is increased. Hence, a reduced maximum current density and transconductance were recorded for large periphery devices, yielding 1.1A/mm and 210mS/mm respectively for the same bias point.

Small signal measurements with the 100x0.3 μ m² device resulted in a f_t of 40GHz and a f_{max} of 78GHz. Additional RF measurements with a 1600x0.3 μ m² device led to a f_t of 41GHz and a f_{max} of 43GHz. These values are suitable for the design of high power amplifier at X- or Ku-band.

On-wafer load pull measurements were performed at 10GHz using a measurement setup with mechanical tuners. No harmonic termination was applied. The 1.6mm device yield an output power of 36.5dBm corresponding to a power density of 2.8W/mm, which is an excellent result for a unpassivated large periphery device. Higher output power levels could be expected by proper passivation of the surface (Eastman et al. (3)). The device was biased

at $V_{ds}=25V$ and $V_{gs}=-4.5V$ leading to a drain current of 230mA (class AB) (figure 4). Self biasing effect pushed the drain current up to almost 500mA. The PAE was approximately 32%. Higher drain-source-voltages could not yet be applied due to a limitation of the currently used DC power source. The breakdown voltage of the device is around 70V.

SMALL SIGNAL ANALYSIS

For large signal modeling of an power amplifier, the knowledge of the small signal FET parameters is very helpful. To distinguish between extrinsic and intrinsic parameters several measurements has to be done. To extract the extrinsic parasitics of the devices, S-parameters at two different bias conditions were measured (pinch-off and large forward gate-bias). For the intrinsic parameters several bias points in the linear and the saturation region were applied. The drain- and source-resistances were determined by DC measurements (proposed by Yang et al.(6)) and by the method of Dambrine et al. and Berroth et al.(4,5). The resistances were extracted from the S-parameters measured for large forward gate bias and fitted to their proposed Z-parasitic topology model. The fitted values, which were evaluated with HPEEsof ADS, were verified with DC-measured values. The inductances were also extracted by this method.

To separate parasitics, which belong exclusively to the pads and the parasitics of the FET itself, gatewidth dependent S-parameter measurements were performed. The pad geometry were kept unchanged and only the gatewidth of the FETs were varied. The derived equations of (4,5) were used to extract the extrinsic parameters of the S-parameters, which were also measured at pinch-off and large forward gate-bias. Afterwards they were plotted against gatewidth and the pad parasitics were extrapolated for zero gatewidth. These values were used as extrinsic constants for the fitting of the intrinsic parameters.

Finally, the S-parameters of the linear and the saturation region of the IV-curve were fitted to a standard small signal equivalent circuit (figure 2) for two different devices, one with the gatewidth of 100 μ m and the other with 1.6mm gatewidth. In figure 3 the measured and the modeled S-parameters are shown for the smaller FET. The figure shows a good agreement between the measured and the modeled data particular in the frequency range of 1 to 25 GHz.

The modeled parameters of both FETs are listed in table 1. The capacitances C_{gs} , C_{ds} , C_{gd} and the transconductance g_m are normalized to 1mm. The capacitances scale quite well with the device size within a range of 10%-40% (intrinsic area ratio: $FET_{large}/FET_{small}=16$). However, the resistive components as well as the transconductance behave non-linearly with size, beyond experimental and/or fitting error, most probably due increased self heating in the larger device. Using the data from small signal equivalent circuit an extrinsic transconductance of 285mS/mm and 230mS/mm for the small and for the large device can be calculated, using $g_{m_{extrin}}=g_{m_{intrin}}/(1+R_s*g_{m_{intrin}})$, in good agreement with the data extracted from DC measurements. For both fittings a source resistance of around 0.5 Ω mm was used.

CONCLUSION

In conclusion, we fabricated small and large periphery devices on s.i. SiC. DC characterization showed state of the art transconductance for a 100x0.3 μ m² device reflecting excellent material properties. S-parameter measurement yield an f_t of 40GHz and f_{max} of 78 GHz for a 100 μ m device. Power measurements shows output power of >4W cw (2.8W/mm) for a unpassivated 1.6mm device at 10GHz. Small signal equivalent circuit parameters have been analyzed for two devices with different gatewidths indicating that a standard equivalent HEMT circuit can be taken to describe AlGaIn/GaN HFETs. However, in order to use this approach to design large periphery devices, we will have to take into account the thermal behavior of the device's components, which do not scale linearly with device size.

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Size	Gm	τ	Cgs	Cgd	Cds	Ri	Rds	Ggs
8x200	268mS/mm	0.7ps	831fF/mm	90fF/mm	181fF/mm	1.6 Ω mm	84 Ω mm	0.42mS/mm
2x50	340mS/mm	0.8ps	880fF/mm	133fF/mm	144fF/mm	0.4 Ω mm	50 Ω mm	1.6mS/mm

Table 1: List of intrinsic small signal parameters. The bias point for the large device and for the small device was $V_{gs}=-4.5V$ and $V_{ds}=10V$.

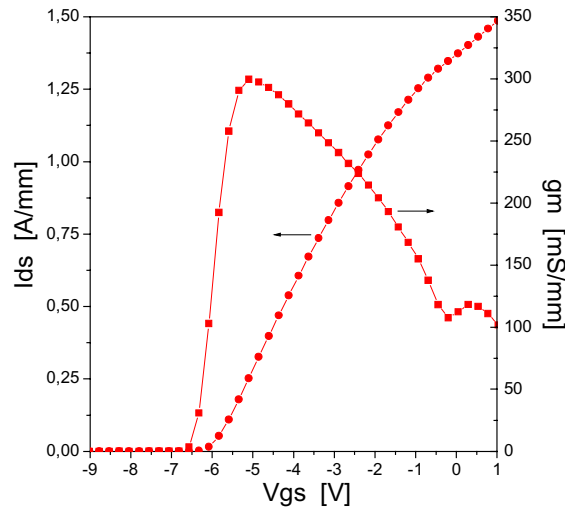


Figure 1: Transfer and transconductance of AlGaIn/GaN HFETs grown on SiC. The measurement was done by $V_{ds}=10V$. Drain current is $I_{ds}=1.5A/mm$ at $V_{gs}=+1V$ and the maximum transconductance is around 300mS/mm.

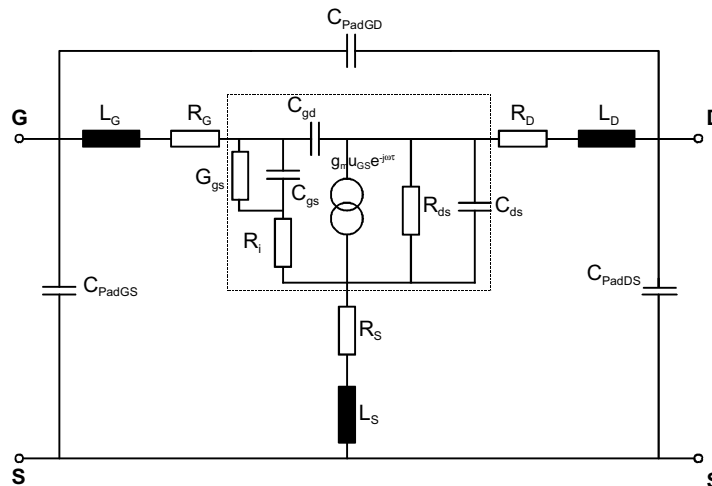


Figure 2: Standard small signal equivalent circuit to which the S-parameters have been fitted.

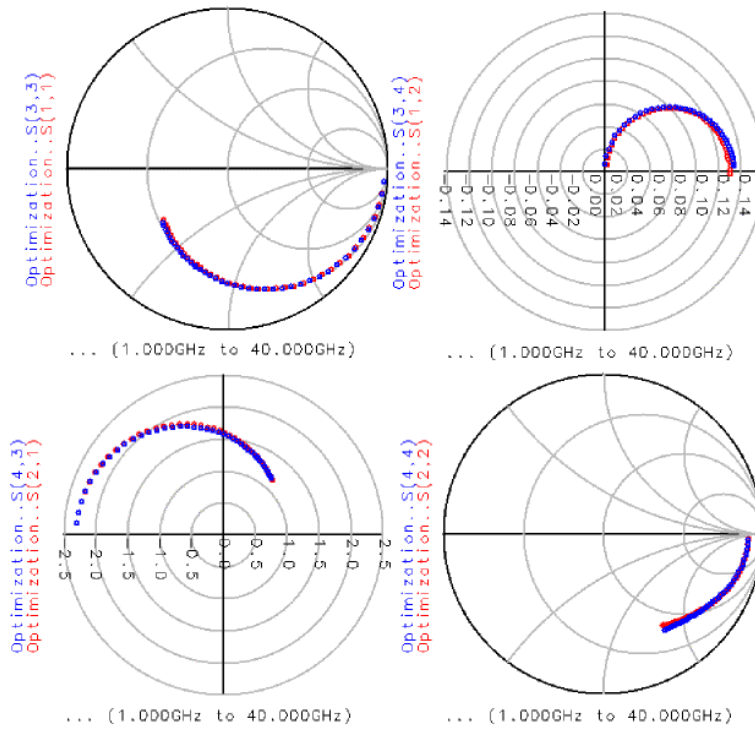


Figure 3: Measured and modeled S-parameters for a 2x50µm HFET biased at $V_{ds}=20V$ and $V_{gs}=-4.25V$

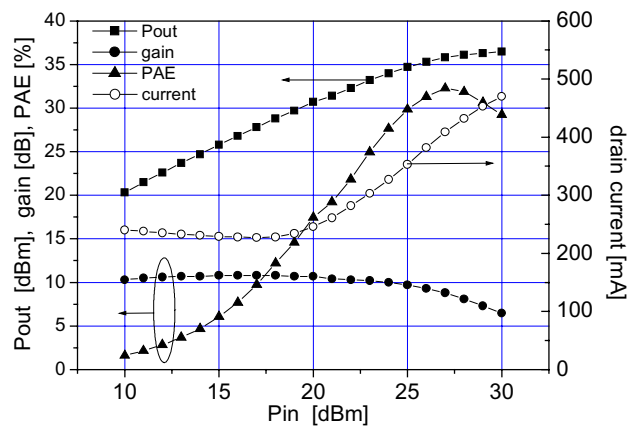


Figure 4: Load pull measurements of the large device at 10GHz biased at $V_{ds}=25V$ and $V_{gs}=-4.5V$ (class AB). $P_{out_{max}}=36.5dBm$, which is 2.8W/mm.