70 GHz F_{MAX} Fully-Depleted SOI MOSFET's for Low-Power Wireless Applications

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Abstract **- For the first time, excellent microwave performances including high frequency noise are reported for 0.25 micron gate channel length Fully Depleted (FD) Silicon-on-Insulator (SOI) MOSFET's: a maximum extrapolated oscillation frequency (f_{max}) of 70 GHz and the state-of-the-art minimum noise figure (NF_{min}) of 0.8 dB with high available associated gain (G_{ass}) of 13 dB at 6 GHz, at V_{ds} = 0.75 V, P_{dc} < 3 mW, have been measured. We demonstrate that the kink related low frequency noise overshoot induced by the floating body effects disappears if the active silicon film thickness is thinned down to 30 nm. Ring oscillators measurements show also that SOI inverters are 30% faster than bulk ones. Finally, the operation at 1.8 V of a sigma delta modulator as well as of critical RF circuits (quadrature generator and mixers) for a zero IF 2 GHz GSM receiver has been demonstrated with this technology.**

I. Introduction

The rapid growth of mobile communication systems leads an increasing request of low cost and low power mixed mode integrated circuits. Maturity of Si-based technology and recent progresses of MOSFET's microwave performances, explain Si success against to III-V technologies for low-power low-voltage wireless applications [1]-[4]. Silicon-on-Insulator-based MOSFET's are very promising devices for multigigahertz applications. Especially low microwave noise at low drain voltage bias condition is one of very interesting high frequency characteristics of such devices. Moreover, due to the reduction of channel length dimension and the improvement of electrode processes (silicidation or metal T-gate processes), very low noise integrated circuits operating beyond 10 GHz and more are realizable. The main goal of this paper is to present state-of-the-art low and high frequency performances of sub-quarter micron gate length FD and PD SOI MOSFET's fabricated with a CMOS-compatible process on low-resistivity (20 Ω.cm) SIMOX wafers. Accurate knowledge of MOSFET noise parameters is required in performing realistic and reliable design of Low Noise Amplifier (LNA), key element of high sensitive microwave receiver. We have accurately determined noise parameters of MOSFET's and we have evaluated their dependence with the fabrication technology. Details about the LETI SOI MOSFET's fabrication process are given in Section II. Static (V_t versus gate length curves and on-off drain current characteristics) and low frequency noise characteristics of FD SOI MOSFET's are presented respectively in Sections III and IV. Propagation delay and DC power consumption of bulk and FD SOI MOSFET's are compared in Section V. Microwave performances including high frequency noise for FD SOI MOSFET's are shown in Section VI. Some results obtained for simple RF functionalities such as a sigma-delta modulator are presented in Section VII.

II. Fully-Depleted SOI CMOS Technology

200 mm UNIBOND wafers with a 400 nm buried oxide are used as the starting material. The active silicon film thickness is thinned down to 40 nm or 30 nm by a recessed-channel process. Gate oxide of 4.5 nm is grown after a LOCOS isolation. A field implant is used to eliminate sidewall leakage. A 200 nm thick polysilicon layer is deposited and patterned by DUV lithography. A medium doped drain implant is followed by formation of a 80 nm spacer oxide after which the source-drain regions are implanted and activated with a 950°C / 15 s RTA. A titanium salicide process is used to reduce the sheet and contact resistances of gates and the elevated 80 nm thick source-drain regions. After the salicide process a gate sheet resistance of about 10 Ω/□, instead of 100 Ω/□ for a classical doped polysilicon gate, is obtained for a 0.25 µm gate channel length MOSFET. The back-end processing includes a three level metal process with W plugs and planarization of intermetal oxides by CMP. Cross-section of a transistor is presented in Fig. 1.

III. MOSFET'S DC CHARACTERISTICS

Fig. 2 shows the threshold voltage V_t roll-off for both FD SOI n and p-MOSFET's. Although V_t is low (about 300 mV at V_{ds} = 0.1 V for 0.25 µm gate length transistors), the off-current at V_{ds} = 1.8 V is only 6 nA/µm and 1 nA/µm for 0.25 µm n and p-MOSFET's, respectively. Fig. 3 presents excellent on-off characteristics (at V_{ds} = 1.8 V) have been measured although the drive current is limited by high series resistance due to the thin silicon under the spacer.

IV. LOW FREQUENCY NOISE PARAMETERS

The floating body effect induces a kink related noise overshoot which adds a Lorentzian spectrum on the flicker noise. This behavior is clearly shown at $V_{gs} \approx V_t$ and V_{ds} = 1 V for devices with a 40 nm active silicon film (t_{si}). But this effect disappears if the active silicon film thickness is thinned down to 30 nm (Fig. 4).

V. PROPAGATION DELAY AND POWER CONSUMPTION

The propagation delay and the power consumption of 90 stages bulk and FD SOI CMOS inverter ring oscillators (FO = 5, W_n = 5 µm, W_p = 10 µm) are shown in Fig. 5. Due to the reduction of the total parasitic equivalent capacitance per gate, the stage delay of the FD SOI inverter is about 30% faster than the bulk one at low power consumption.

VI. HIGH FREQUENCY CHARACTERIZATION

S and noise parameters have been measured using a HP8510 network analyzer, a HP8971 noise measurement set-up and tungsten contact Picoprobe microwave probes. The S-parameters were measured up to 40 GHz and the noise figures in the 1-18 GHz frequency range. The four noise parameters are obtained using the NF50 method [5]. A current gain cut-off frequency f_T close to 40 GHz at V_{gs} = V_{ds} = 1 V has been measured for 0.25 µm FD SOI n-MOSFET with a current density of 100 mA/mm (see Fig. 6). For the same bias conditions, an extrapolated (from –20 dB/dec slope) maximum oscillation frequency f_{max} of 70 GHz has been obtained. This result is one of the best results reported in the literature today for MOSFET's. Those high frequency performances are the result of low capacitances (gate-drain and drain-source capacitances) of the optimized SOI MOSFET's structure and the reduced gate resistance by using the salicide process. Knowing the 3-D physical structure of built MOSFET's, direct extraction techniques have been developed to accurately characterize sub-quarter micron SOI MOSFET's in the microwave domain [6]. The characterization procedure is directly based on the physical meaning of each small-signal model element. That makes it very useful for controlling the sensitive fabrication steps such as the silicidation process of the gate, source and drain regions.

Accurate knowledge of transistor noise parameters is required in performing realistic and reliable design of Low Noise Amplifier (LNA), key element of high sensitive microwave receiver. All the experimental results, presented in this paragraph, correspond to SOI FD n-MOSFET's composed of 12 parallel-connected gate fingers of 0.25 µm channel length and 6.6 µm width (noted 12x6.6x0.25 µm²). Fig. 7 shows the variation, at 2 GHz, of the NF_{min} and G_{ass} as a function of the drain current density (V_{ds} = 2 V). For a drain current density close to 60-70 mA/mm, the NF_{min} is close to 0.4 dB with G_{ass} of 21 dB. Fig. 8 represents the state-of-the-art results for different kinds of MOSFET's technologies. Low noise microwave performances of FD SOI MOSFET's appear to be ones of the best results reported in the literature. Fig. 9 shows the variation of NF_{min} and G_{ass} as a function of drain power density (V_{ds} = 0.75 V) at higher frequency (6 GHz). For a drain power density close to 25-30 mA/mm, NF_{min} is about 0.8 dB and G_{ass} is close to 13 dB. NF_{min} does not increase too much by decreasing V_{ds}. These results show that LNA's could be designed with a power consumption of less than 35 mW/mm.

VII. ANALOG AND RF CRITICAL BLOCKS FOR A GSM RECEIVER

The functionality of baseband circuits, including a delta-sigma modulator (see specifications in Table I) as well as a quadrature generator (gain and phase accuracy demonstrated at 2 GHz with a 1.8 V supply voltage) and mixers has been demonstrated with the FD SOI technology, without the use of the salicide process (N+ single gate instead of dual gates). In this case f_{max} is reduced to about 30 GHz at V_{gs} = V_{ds} = 0.9 V but these performances are still sufficient for a 1.8 GHz receiver. Better performances at lower voltage supply and power consumption can be expected by using salicided transistors.

VIII. CONCLUSION

We have performed a complete study of low and high frequency characteristics including noise figures for a 0.25 µm FD SOI MOSFET. These transistors show a NF_{min} of about 0.8 dB and a G_{ass} of 13 dB at 6 GHz. Using such devices, it should be possible to design a LNA with a noise figure less than 3 dB and 15 dB of gain at 12 GHz. By decreasing furthermore the gate resistance (by improving the salicide process or by using a T-gate), such performances could be obtained at 18 GHz for the same gate length. Moreover, as performances on digital circuits show a high speed with a low power consumption compared to bulk devices, such SOI devices could be used for wireless applications where high frequency as well as high speed/low power is required in RF and digital parts, respectively.

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	Measured	Spec.
Analog Input bandwidth	100 kHz	100 kHz
Analog sampling rate	13/2 MHz	13/2 MHz
Signal/Noise ratio	70-75 dB	> 78 dB
Total Harmonic Distorsion	70-85 dB	> 40 dB
Power supply	1.6 V-2 V	1.6 V-2 V

Table I. Baseband circuit specifications.

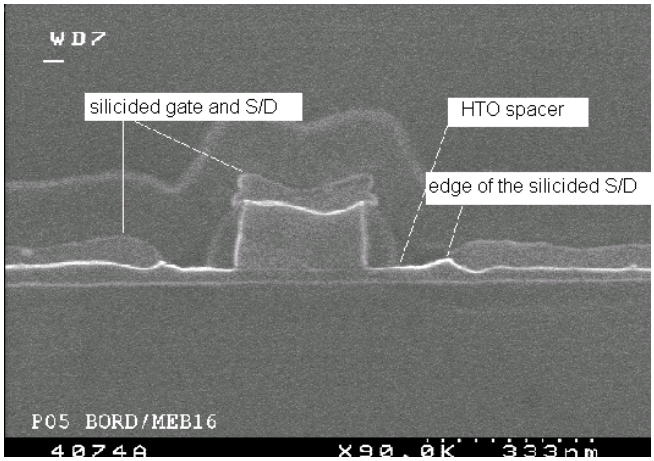

Fig. 1. Cross-section of a salicided 0.25 µm FD SOI MOSFET.

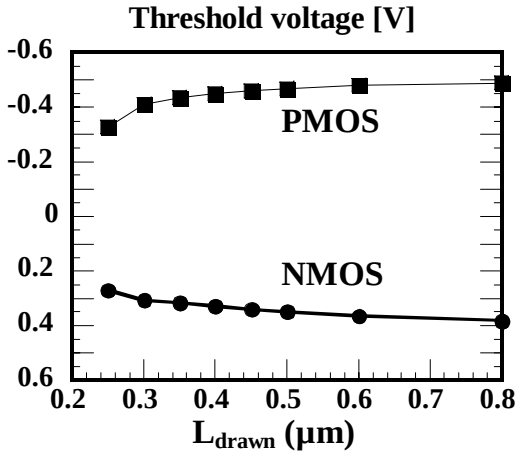

Fig. 2. V_t versus gate length at V_{ds} = 0.1 V.

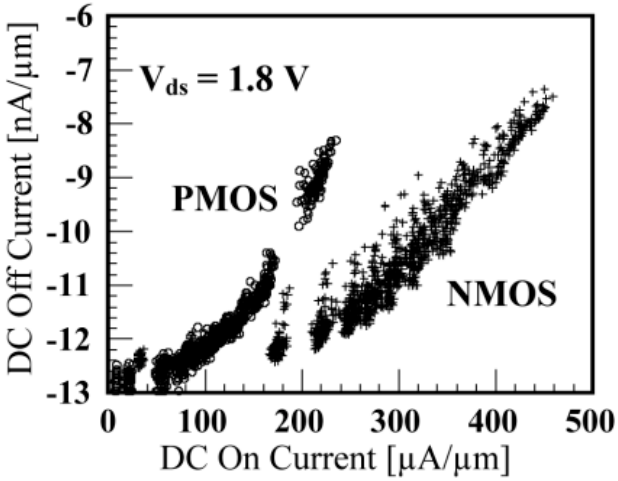

Fig. 3. On-off characteristics at V_{ds} = 1.8 V.

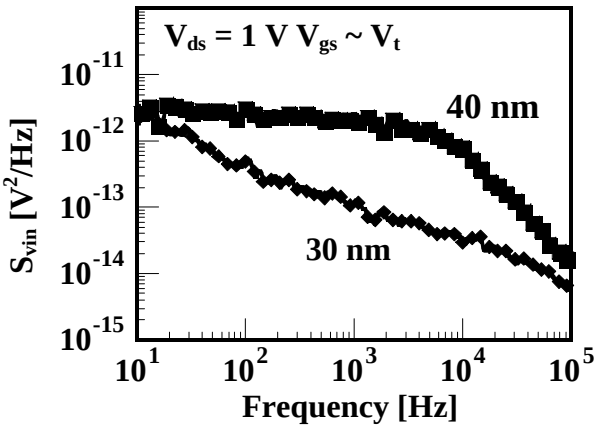

Fig. 4. LF noise versus frequency at $V_{gs} \approx V_t$, V_{ds} = 1 V; NMOS, L_g = 0.25 µm, W = 25 µm, t_{si} = 30 or 40 nm.

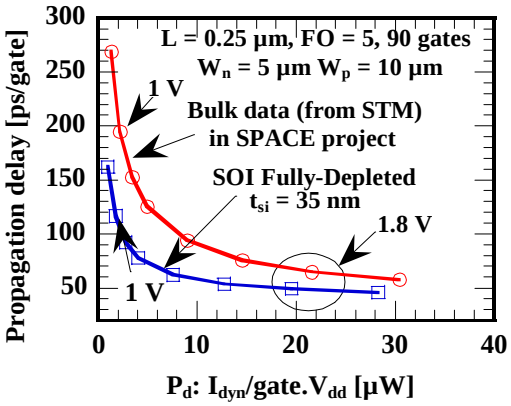

Fig. 5. Propagation delay versus power consumption.

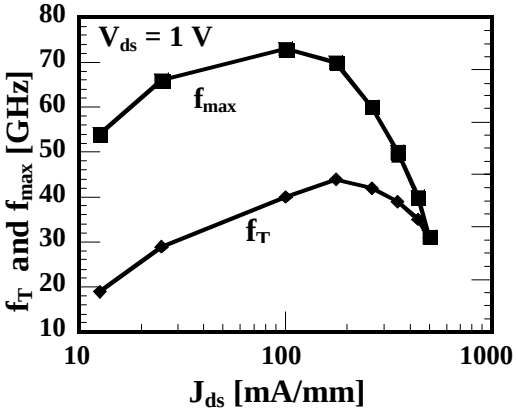

Fig. 6. f_T and f_{max} versus current density, V_{ds} = 1 V; $nxWxL_g$ = 12x6.6x0.25 µm^2.

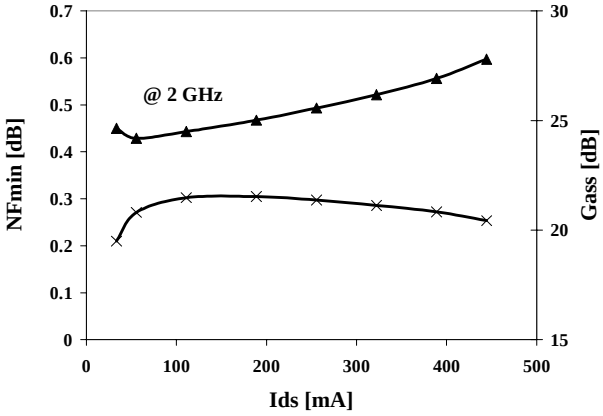

Fig. 7. FD SOI MOSFET's evolution of NF_{min} (▲) and G_{ass} (x) as a function of the drain current density at 2 GHz; V_{ds} = 2 V; $nxWxL_g$ = 12x6.6x0.25 µm².

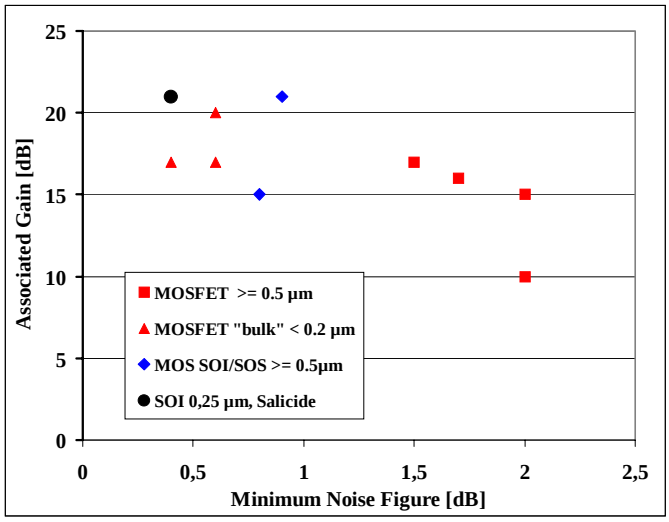

Fig. 8. State-of-the-art high frequency NF_{min} and G_{ass} for different published results of MOSFET technologies. Black dot corresponds to this work.

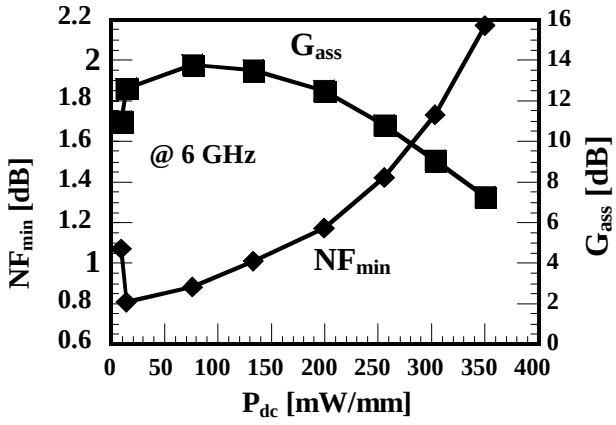

Fig. 9. NF_{min} and G_{ass} versus power consumption at 6 GHz; V_{ds} = 0.75 V; $nxWxL_g$ = 12x6.6x0.25 µm^2.