A Simplified Thermal Analysis Approach for Power Transistor Rating in PWM-Controlled DC/AC Converters

Fabio Filicori and Corrado Guarino Lo Bianco

***Abstract*— A simplified dynamic thermal analysis approach is proposed for the estimation of the peak junction temperature in power IGBT transistors operating in pulse-width modulation (PWM) controlled DC/AC converters. This approach can be used for the rating of electron devices or heatsink systems in power circuit design, as it provides a direct analytical link, in terms of electrical and thermal device parameters and converter operating conditions between the case and the peak junction temperatures. In this way, by imposing a given upper limit on the junction temperature, indirect constraints on device size or load current or heatsink efficiency can easily be obtained. The approach is based on mild, pessimistic approximations on both the spectrum of dissipated power and on the dynamic thermal behavior of the device. The validity of such approximations has been verified by comparison with the results of accurate numerical simulations carried out by using measurement-based loss models. Possible ways of using this approach in a converter rating context are outlined in the paper, by considering different design scenarios.**

***Index Terms*— IGBT, power converters, power device rating, thermal analysis.**

NOMENCLATURE

The symbol $\hat{}$, when placed above a variable, denotes its peak value. The superscript LF points out a time-domain averaging (like the well-known state-space averaging), carried out on a variable by using a moving time-window, while superscript LIM indicates the maximum admissible value of a variable for safe operation. The subscript 0 indicates the mean value of a variable, while RMS indicates its root mean square value. Lower case variables represent time-varying quantities (for example i is time varying while $I_{\rm RMS}$ is time invariant).

$C_j,\ R_{jc}$	Junction thermal capacitance, junction-to-case thermal static resistance.
$\tau,\ f_\theta$	Junction-to-case thermal time constant and thermal cut-off frequency.
$\theta_j,\ \theta_C$	Junction and case temperatures.
p_T	Transistor's instantaneous power losses.
$\tau_{\rm EQ}$	Equivalent commutation time for loss estimation.
$V_{\rm IN}$	Power converter feeding voltage.
i, v	Power converter output current and voltage.
T, f	Period and frequency of the output voltage.
T_C, f_C	Commutation period and frequency of the power converter.
ρ	Instantaneous duty-cycle in PWM operation.
$E_{\rm off}, E_{\rm on}$	Turn-off and turn-on energy losses.
$\tau_{\rm off}, \tau_{\rm on}$	Turn-off and turn-on times.
p_T^c, p_T^r	Transistor instantaneous switching and conduction losses.
$V_{ce}^{\rm SAT}$	Transistor saturation voltage.
$\cos(\varphi), a$	Output current phase shift and output modulation index.

Manuscript received January 8, 1996; revised May 21, 1996 and August 5, 1997. This paper was recommended by Associate Editor A. Ioinovici.

F. Filicori is with the Department of Electronics, Computers and Systems Science, University of Bologna, 40136 Bologna, Italy.

C. Guarino Lo Bianco is with the Dipartimento di Ingegneria dell'Informazione, University of Parma, 43100 Parma, Italy.

Publisher Item Identifier S 1057-7122(98)02531-8.

I. INTRODUCTION

THERMAL analysis is a fundamental issue in power converter design, since the most convenient choice of the switching power device and associated heatsink are both strictly related to the basic requirement of keeping the junction temperature below the maximum admissible value. To this aim, electrical loss models, that provide an estimate of power losses (i.e., heat generation) in terms of electrical operating conditions, are needed. Moreover, a thermal model and an associated thermal analysis procedure must also be used to estimate the "worst-case" peak value of the junction-to-case temperature drop.

A number of loss models, including both conduction and switching losses (i.e., turn-on and turn-off loss energies) have been proposed in the literature [1]–[8]. These enable to estimate the time-dependent transistor dissipated power $p_T(t)$ for given driving signals and electrical operating conditions (i.e., both in "hard" inductive or resistive switching [1], [4], [5], [7]–[9], [11], or "soft" switching when quasiresonant topologies or other special-purpose circuits are used [6], [10]) on the basis of device parameters available on data-sheets. Sometimes, experimental data provided by device manufacturers (e.g., graphs providing $V_{ce}^{\rm SAT}$ and switching loss energies as functions of current, voltage and temperature) can be directly used, for this purpose, as look-up table models. By using these available models the average transistor dissipated power P_{T0} can be computed [1], [4]–[11] and, consequently, the average junction-to-case temperature drop $\theta_{j0} - \theta_C$ can be estimated in terms of junction-to-case thermal resistance R_{jc} [4]–[6]. On this basis, for converter operating conditions that involve negligible "ripple" in the junction temperature, a correct, thermally safe design (i.e. combined heatsink and power transistor rating) can easily be carried out [4], [5]. This happens when output fundamental frequencies are much higher

than the cut-off frequency associated to thermal dynamics (e.g., in DC/DC or DC/AC converters with relatively high output frequencies and fast switching devices). Unfortunately, this is not true for DC/AC converters operating with output frequencies that are comparable with, or even smaller than, the transistor thermal cut-off frequency (e.g., variable frequency AC motor drives). In such conditions, the peak value $\hat{\theta}_j - \theta_C$ of the junction-to-case temperature, which can be much greater than its mean value $\theta_{j0} - \theta_C$, must be correctly estimated for thermally safe design. To this aim, one of the many dynamic thermal models available in the literature, possibly including nonuniform temperature distributions, could be used [9]. However, because converter circuit design should be mainly based on commonly available device data, a linear first-order model, which practically coincides with the thermal characterization provided by all device manufacturers, should be used. Yet, even when using this simple model, dynamic thermal analysis of pulse-width modulation (PWM) controlled DC/AC converters is not a trivial task, owing to the complex shape and spectrum of electrical variables. Up to now, this problem has been faced by using numerical simulation techniques [9], that may provide sufficiently accurate results, but are not suitable for a first tentative design procedure owing to their complexity.

In this paper, a fully analytical, simplified approach, that provides a slightly pessimistic estimate for $\hat{\theta}_j - \theta_C$ is proposed. The peak thermal drop is evaluated in terms of the commonly available device data and converter operating conditions and can be conveniently used to guarantee thermally safe operating conditions in PWM–controlled converters, since it provides simple criteria for transistor selection and heatsink rating.

In the following IGBT transistors, which are at present the most commonly used power devices for such applications, will be considered. However, it should be noted that our thermal analysis approach and associated "worst-case" approximations are valid in any case. In practice, for IGBT's the temperature estimate will be sufficiently accurate, while more pessimistic results could be obtained for other types of devices. The topology of the power converter considered in this paper is shown in Fig. 1. The proposed approach can be applied to either a three-phase or to a single-phase converter. The same commutation law, except for the associated time-shifts, is assumed for all the "legs" of the converter. The load is assumed to be balanced. The previous hypotheses simplify the thermal analysis since, under such conditions, all the "legs" are subject to the same thermal stresses. For this reason, only one "leg" of the converter is considered. In the same way, we assume that both transistors of each "leg" operate under the same electrical and thermal stresses. Thus, only one transistor for each "leg" is considered for thermal analysis (in the following T_1 will be chosen). Almost all commutation laws satisfy these conditions. Otherwise, if the thermal or the electrical conditions are different for the two devices, the same procedure should be applied to each transistor separately.

In Section II, an approximation for the spectrum of the power losses is proposed to simplify the thermal analysis. In Section III, the thermal dynamic behavior of the power transistor is investigated by means of a simplified, "worst-case" analytical approach. In Section IV, the transistor time-dependent dissipated power is expressed in terms of the given converter operating conditions and electrical transistor characteristics. On this basis, in Section V the peak and the mean values of power losses are computed by considering PWM sinusoidal modulations both with and without third harmonic distortion. In Section VI some practical applications of the proposed method are discussed by considering different transistor and heatsink selection problems under the constraint of thermally safe operation. Finally, in Section VII, the transistor peak temperature estimated according to our "worst-case" analytical approach is compared with the results of numerical simulations carried out by using measurement-based loss models.

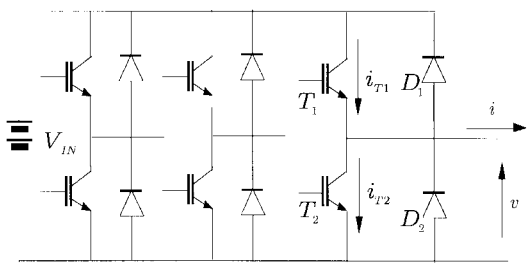

Fig. 1. Electrical scheme of a three phase DC/AC converter.

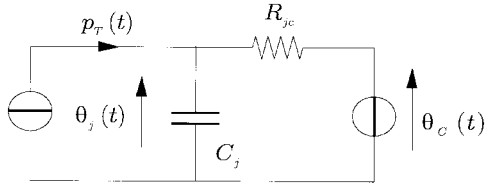

Fig. 2. Electrical scheme equivalent to the junction thermal equation of an electronic device.

II. Spectral Approximation for a Simplified Thermal Analysis

Electron device and heatsink rating for the design of power converter circuits necessarily involves a thermal analysis. To this aim, the simple dynamic thermal model shown in Fig. 2, which exactly corresponds to the thermal characterization provided by most device manufacturers, is used. This model represents the junction temperature θ_j in terms of the static junction-to-case thermal resistance R_{jc} and the thermal time constant $\tau = R_{jc}C_j$. Clearly, this is a simplified model because it does not take into account the nonuniform internal device temperature. However, since device selection and circuit design are normally carried out exclusively on data provided by manufacturers, this is the only scheme that can be practically used.

Under PWM operating conditions, the thermal analysis of an electron device, even when using the simple model in Fig. 2, is quite complicated owing to both the dynamics involved and the complex spectrum of the electrical variables. However, the analysis can be greatly simplified since, according to this model, the device thermal transfer function $H(s)$ is of a low-pass type with a cut-off frequency $f_\theta = 1/2\pi\tau$ (with

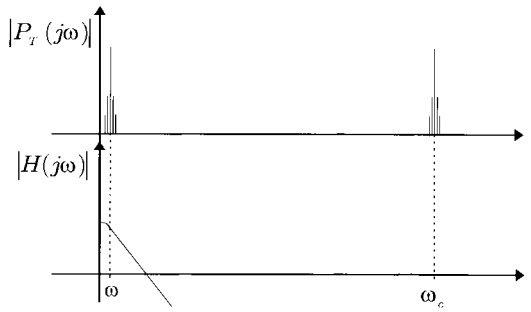

Fig. 3. Spectrum of the power losses and module of $H(j\omega)$.

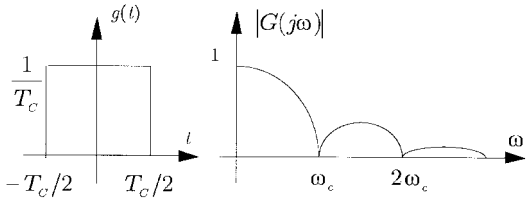

Fig. 4. Equivalent pulse response $g(t)$ and associated module of transfer function $G(j\omega)$ corresponding to the averaging operator (1).

$\tau = R_{jc}C_j$) which is comparable[1] with the converter output fundamental frequency f, but much lower than the PWM switching frequency f_C. In such conditions only the lower part (see Fig. 3) of the spectrum of $p_T(t)$ is significant for thermal analysis, while its high-frequency components can be neglected. Thus, in temperature analysis the instantaneous dissipated power $p_T(t)$ can be replaced by its corresponding "low frequency" part $p_T^{\mathrm{LF}}(t)$ defined as

$$p_T^{\mathrm{LF}}(t) \triangleq \frac{1}{T_C}\int_{t-T_C/2}^{t+T_C/2} p_T(\tau)\, d\tau \tag{1}$$

where the time-averaging operation over a moving time-interval T_C corresponds to a low-pass filtering whose associated module of transfer function $G(j\omega)$ and pulse response $g(t)$ are schematically shown in Fig. 4.

It can be noted that the time-averaging operator in (1) attenuates all the high-frequency harmonics. In particular, it almost completely cuts off the harmonics close to the multiples of the commutation frequency f_C. If this operator is used to prefilter the power losses $p_T(t)$, according to the scheme in Fig. 5, the resulting signal $\theta_j^{\mathrm{LF}}(t)$ can be considered to be substantially equal to the signal $\theta_j(t)$ obtained directly from $H(s)$ (see Fig. 6). In fact, the low frequency harmonics are not influenced by the presence of an operator like that in (1), while the highest ones are, in any case, cut off by the action of $H(s)$.

This consideration leads to using $p_T^{\mathrm{LF}}(t)$, instead of $p_T(t)$, to estimate the junction temperature. The handling of signals with simpler shapes and spectra is an obvious advantage of this procedure.

[1] For silicon power devices, the thermal time constant τ, which can be easily derived from the dynamic thermal response graphs provided in data-sheets, is typically in the range 15–70 ms. Thus, the corresponding thermal cut-off frequency is normally lower than $\approx$10 Hz.

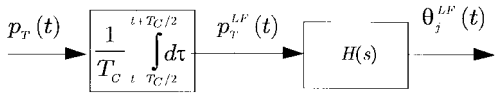

Fig. 5. Estimation of the junction temperature.

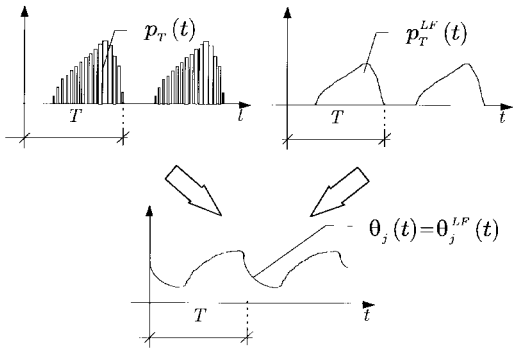

Fig. 6. The time shape of the junction temperature does not depend on the high-frequency harmonics of the power spectrum.

III. Simplified Dynamic Analysis for the Estimation of the Junction Peak Temperature

Since typical applications of power DC/AC converters involve output frequencies f which are comparable or even lower than the thermal cut-off frequency of power devices (e.g., variable frequency motor-drives), a time-varying periodic solution of the equation

$$p_T^{\mathrm{LF}}(t) = C_j\frac{d\Delta\theta(t)}{dt} + \frac{\Delta\theta(t)}{R_{jc}} \tag{2}$$

which corresponds to the model in Fig. 2 with $\Delta\theta(t) = \theta_j(t) - \theta_c$, must be found. In line with the previous considerations, $p_T^{\mathrm{LF}}(t)$ has been used instead of $p_T(t)$. In particular, solving (2) for its periodic solution, leads to

$$\Delta\theta(t) = \frac{1}{1-e^{-(T/\tau)}}\,\frac{1}{C_j}\int_{t-T}^{t} p_T^{\mathrm{LF}}(\beta)e^{-[(t-\beta)/\tau]}\, d\beta. \tag{3}$$

Equation (3) could be used for the maximum current rating of a given device in a given converter, by imposing an upper limit θ_j^{LIM} on the peak temperature $\hat{\theta}_j$ and expressing the transistor power losses $p_T(t)$ as functions of the operating conditions (see Section IV). In practice, this is a difficult task both because (3) involves an integral computation on a waveform $p_T^{\mathrm{LF}}(t)$ that is still complex and, moreover, because the maximum value of the time dependent quantity $\Delta\theta(t)$ must be found.

However, in view of device/heatsink rating for converter design, this problem can be overcome by introducing a suitable, easy-to-use "pessimistic" estimate of $\hat{\theta}_j$. In particular, the peak temperature drop $\Delta\hat{\theta}$ can be estimated with reasonable accuracy (see Appendix A) through the "pessimistic" approximating function

$$\Delta\hat{\theta} \le \Psi \triangleq R_{jc}\hat{P}_T^{\mathrm{LF}}\frac{1-e^{-(P_{T0}/\hat{P}_T^{\mathrm{LF}})(T/\tau)}}{1-e^{-(T/\tau)}}. \tag{4}$$

Equation (4) is much easier to use than (3), because it does not involve a complete knowledge of the shape of $p_T^{\mathrm{LF}}(t)$

and, moreover, it does not require any integration. In fact, (4) directly provides an estimation of the maximum value $\Delta\hat{\theta}$ in terms of the mean value

$$P_{T0} = \frac{1}{T}\int_0^T p_T^{\mathrm{LF}}(t)\,dt \tag{5}$$

and the peak value

$$\hat{P}_T^{\mathrm{LF}} = \max_t\{p_T^{\mathrm{LF}}(t)\} \tag{6}$$

of the low-frequency part of dissipated power. As is shown in Appendix A, this result is achieved whatever the shape of $p_T^{\mathrm{LF}}(t)$. This property directly derives from the presence of a monotonically decreasing "weight" $e^{-(t/\tau)}$ applied to $p_T^{\mathrm{LF}}(t)$ in the integral of (3).

The reasonable accuracy of (4), which will be validated through the numerical examples given in Section VII, can be qualitatively understood by considering that (4) is exact when the operating frequency f is much higher or much smaller than the thermal cut-off frequency f_θ. In fact, when $f \gg f_\theta$, (4) gives $\Delta\hat{\theta} \cong R_{jc}P_{T0}$, which is clearly correct; on the other hand, in the complementary case $f \ll f_\theta$, it gives the correct result $\Delta\hat{\theta} \cong R_{jc}\hat{P}_T^{\mathrm{LF}}$.

Equation (4) can also be written as

$$\Delta\hat{\theta} = \tilde{R}_{jc}\hat{P}_T^{\mathrm{LF}} \quad \text{with } \tilde{R}_{jc} = R_{jc}\frac{1-e^{-(P_{T0}/\hat{P}_T^{\mathrm{LF}})(T/\tau)}}{1-e^{-(T/\tau)}} \tag{7}$$

which practically coincides with the so-called transient thermal impedance $\tilde{R}_{jc}$ normally provided on manufacturers' data-sheets. This shows that the measured transient thermal impedance can be practically used not only in the case of single square-pulse periodic operation, but also in a much more general context, provided that the low-frequency approximation on $p_T(t)$ is introduced.

IV. Simplified Computation of the Peak and of the Mean Values of the Transistor Losses

In order to use (7) for device rating or heatsink design purposes, $\hat{P}_T^{\mathrm{LF}}$ and P_{T0} must be expressed in terms of the converter operating conditions. To this aim, according to commonly used approaches, $p_T(t)$ is written as the sum of two different terms

$$p_T(t) = p_T^r(t) + p_T^c(t) \tag{8}$$

where $p_T^r(t)$ and $p_T^c(t)$ are, respectively, the so-called conduction (i.e., "Resistive") and switching (i.e. "Commutation") losses. In particular, the resistive part can be expressed as

$$p_T^r(t) = V_{ce}^{\mathrm{SAT}} i_T(t). \tag{9}$$

The second term $p_T^c(t)$ consists of a sequence of short-duration large-amplitude pulses (see Fig. 7). For thermal analysis purposes, only pulse areas (i.e., turn-on and turn-off energies) are relevant.

As stated in Section II, thermal analysis can be performed by taking into account only the low-frequency spectral components of the power losses; thus $p_T^{c\text{-}\mathrm{LF}}(t)$ can be used instead

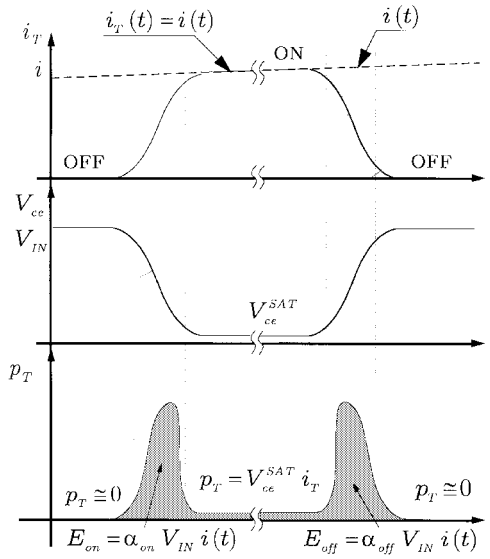

Fig. 7. Qualitative representation of the commutation cycle of an IGBT transistor: (a) current shape, (b) voltage shape, and (c) instantaneous power dissipation shape.

of $p_T^c(t)$ and $p_T^{r\text{-}\mathrm{LF}}(t)$ instead of $p_T^r(t)$. In particular

$$p_T^{r\text{-}\mathrm{LF}}(t) \triangleq \frac{1}{T_C}\int_{t-T_C/2}^{t+T_C/2} V_{ce}^{\mathrm{SAT}} i_T(\tau)\,d\tau = V_{ce}^{\mathrm{SAT}}\frac{1}{T_C}\int_{t-T_C/2}^{t+T_C/2} i_T(\tau)\,d\tau. \tag{10}$$

In (10), for simplicity's sake, V_{ce}^{SAT} has been considered as a constant. Actually, in IGBT's it mildly increases versus current [see, e.g., Fig. 11(b)]. Thus, in view of "safe" device rating (i.e., pessimistic worst-case analysis) the constant value of V_{ce}^{SAT} should be chosen corresponding to the peak load current. This leads to temperature estimation which is not too pessimistic, since the largest amount of conduction losses is produced when the output current is larger. Temperature dependence of V_{ce}^{SAT} in IGBT devices is very weak and normally increases in the high current range.[2] Thus, assuming *a priori* a constant V_{ce}^{SAT}, corresponding to the maximum allowable temperature, is not too pessimistic for correct device/heatsink rating, because the errors introduced will be of some importance only when the actual operating temperature is much lower than the given limit θ_j^{LIM}.

The transistor current $i_T(t)$ can be directly expressed in terms of the converter output current $i(t)$. In fact, the upper transistor of each "leg" (similar considerations hold also for the lower one), is crossed by the output current only if this is positive and the device is in the "ON" state. This situation is shown in Fig. 8 and can be expressed analytically as

$$i_T(t) = \frac{i(t)+|i(t)|}{2}m(t) \tag{11}$$

where $m(t)$ symbolically represents the driving signal ($m = 0, 1$ corresponds, respectively, to "OFF/ON" states). The pres-

[2] This happens since the voltage drop across the series equivalent resistance, which is not negligible at high currents, has intrinsically a positive temperature coefficient owing to carrier mobility reduction.

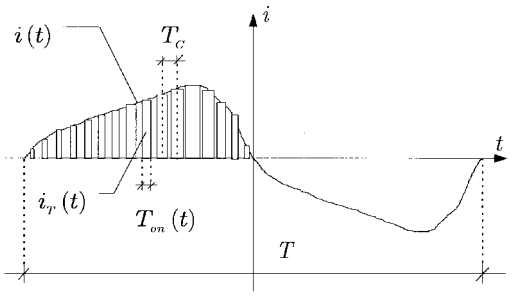

Fig. 8. Currents shape in a power converter. The solid line indicates the output current, while pulses refer to the current flowing through the upper transistor. For a commutation frequency much higher than the output frequency, the transistor current can be considered constant during each conduction period.

ence of loads with series inductance strongly limits the variability of the output current so that, if $f_C \gg f$, the output current can be considered to be almost constant during each switching period. Thus, taking (10) and (11) into account, we obtain

$$p_T^{r\text{-LF}}(t) = V_{ce}^{\text{SAT}} \frac{i(t)+|i(t)|}{2} \frac{1}{T_C} \int_{t-T_C/2}^{t+T_C/2} m(\tau)\, d\tau. \quad (12)$$

Then, the conduction losses can be expressed as

$$p_T^{r\text{-LF}}(t) = V_{ce}^{\text{SAT}} \rho(t) \frac{i(t)+|i(t)|}{2} \quad (13)$$

where

$$\rho(t) \triangleq \frac{1}{T_C} \int_{t-T_C/2}^{t+T_C/2} m(\tau)\, d\tau$$

is the instantaneous duty-cycle.

In order to estimate $p_T^{c\text{-LF}}(t)$ the energies E_{on} and E_{off}, lost, respectively, at any transistor turn-on and turn-off, must be computed. To this aim, various models have been proposed in the literature [2]–[7], that enable for switching energy estimation in terms of switched current, voltage, temperature, and operating conditions. In this paper, for the sake of simplicity and with reasonable approximation, we assume that E_{on} and E_{off} can be considered to be almost proportional to both the converter supply voltage V_{IN} and the switched current [i.e., the load current $i(t)$ when $i(t) > 0$]. Thus, switching losses can be expressed, at any time t, as

$$E_{\text{on}} = \alpha_{\text{on}} V_{\text{IN}} \frac{i(t)+|i(t)|}{2}$$
$$E_{\text{off}} = \alpha_{\text{off}} V_{\text{IN}} \frac{i(t)+|i(t)|}{2}. \quad (14)$$

This is clearly an approximation, since E_{on} and E_{off} are not strictly proportional to V_{IN} and, above all, $i(t)$. However, according to both manufacturers' data and experimental results provided by other authors [3]–[5], [12], a linear approximation of inductive switching losses versus $i(t)$ is quite reasonable [see, e.g., Fig. 11(a)]. Voltage dependence, on the other hand, is much less important in a DC/AC converter (where the switched voltage normally coincides with the almost constant input supply voltage) and, in any case, can also be approximated by a linear function. Thus, (14) can give a reasonable estimate of the switching energies E_{on} and E_{off} provided that suitable values are chosen for the coefficients α_{on} and α_{off} (or more precisely for their sum $\tau_{\text{EQ}} = \alpha_{\text{on}} + \alpha_{\text{off}}$). These can be derived, for instance, by "least-square" fitting of (14) to the conventional manufacturer graphs (or other analytical loss models [4]) providing total switching losses versus current, voltage, and temperature. However, a "worst-case," pessimistic choice (i.e., a constant τ_{EQ}, corresponding to $E_{\text{on}} + E_{\text{off}}$, at the maximum load current[3] and maximum admissible θ_j^{LIM}) is preferable in view of safe device/heatsink rating. This, again, leads to results that are not too pessimistic for rating purposes, since larger errors can be expected only under operating conditions which are well away the limits of safe operation.

The switching losses $p_T^c(t)$ are made up of a series of pulse pairs (the first one refers to the device turn-on while the second one to the device turn-off) having a large amplitude but a relatively short length ($\tau_{\text{on}}, \tau_{\text{off}} \ll T_C$). For this reason, in order to evaluate $p_T^{c\text{-LF}}(t)$, only the area $(E_{\text{on}}, E_{\text{off}})$, but not the shape, of each single pulse is important. If an almost stationary PWM modulation is assumed (i.e., $f \ll f_C$), only two pulses are present in each commutation period. As a consequence, $p_T^{c\text{-LF}}(t)$ can be considered approximately stationary along T_C, so that the low-frequency components of $p_T^c(t)$ can be expressed as

$$p_T^{c\text{-LF}}(t) = \frac{1}{T_C} \int_{t-T_C/2}^{t+T_C/2} p_T^c(\tau)\, d\tau = \frac{1}{T_C} \tau_{\text{EQ}} V_{\text{IN}} \frac{i(t)+|i(t)|}{2} \quad (15)$$

where $\tau_{\text{EQ}} = \alpha_{\text{on}} + \alpha_{\text{off}}$.

Finally, the total instantaneous low-frequency power losses $p_T^{\text{LF}}(t)$ are given by the sum of the conduction and the switching losses

$$p_T^{\text{LF}}(t) = p_T^{c\text{-LF}}(t) + p_T^{r\text{-LF}}(t)$$
$$= \left[f_C \tau_{\text{EQ}} V_{\text{IN}} + V_{ce}^{\text{SAT}} \rho(t) \right] \frac{i(t)+|i(t)|}{2}. \quad (16)$$

In the following section, power losses $\hat{P}_T^{\text{LF}}$ and P_{T0}, to be used in (4), will be computed according to (16).

V. Evaluation of the Peak and the Mean Values of the Power Losses for Conventional Modulation Laws

Equation (4) can be used to deal with different problems arising in the thermal rating of power transistors for the design of PWM-controlled converters under dynamic operating conditions (i.e., time varying duty-cycle ρ). To this aim, both the peak low-frequency $\hat{P}_T^{\text{LF}}$ and the mean value P_{T0} of the power losses must be estimated according to (16) for a given load. In the following, DC/AC converters driving linear loads with series inductance will be considered. Both purely

[3] In high-voltage, high-current IGBT's, losses are normally increasing functions of switched current and temperature.

sinusoidal and sinusoidal with third harmonic predistortion (PWM) modulation laws will be considered. In particular, our analytical approach will be used to compare these waveforms from the point of view of transistors thermal stresses. The same procedure can be extended to other modulation laws. The instantaneous duty-cycle for a sinusoidal modulation can be expressed as

$$\rho(t) = \frac{1}{2} + \frac{a}{2}\sin\left(\frac{2\pi}{T}t\right) \tag{17}$$

where a is the modulation index which depends on the RMS voltage required by the load.

For a high-efficiency converter with sinusoidal modulation, possibly including also third harmonic distortion, a is given by (see Appendix B)

$$a \cong \frac{2\sqrt{2}V_{\mathrm{RMS}}}{V_{\mathrm{IN}}}. \tag{18}$$

When a sinusoidal PWM modulation is adopted with fast switching devices and the load is linear and inductive, an almost sinusoidal output current with a given phase delay φ has to be expected under periodic steady-state conditions:

$$i(t) = I_{\mathrm{RMS}}\sqrt{2}\,\sin\left(\frac{2\pi}{T}t - \varphi\right). \tag{19}$$

By substituting (17) and (19) into (16) and after a few algebraic manipulations, we obtain

$$p_T^{\mathrm{LF}}(t) = \begin{cases} \left[\alpha_1 + \alpha_2 \sin\left(\dfrac{2\pi}{T}t\right)\right]\sin\left(\dfrac{2\pi}{T}t - \varphi\right), \\ \qquad \text{when } \sin\left(\dfrac{2\pi}{T}t - \varphi\right) > 0 \\ 0, \qquad \text{when } \sin\left(\dfrac{2\pi}{T}t - \varphi\right) \le 0 \end{cases} \tag{20}$$

where

$$\alpha_1 = \sqrt{2}I_{\mathrm{RMS}}\left(f_C V_{\mathrm{IN}}\tau_{\mathrm{EQ}} + \frac{V_{ce}^{\mathrm{SAT}}}{2}\right)$$

and

$$\alpha_2 = \sqrt{2}I_{\mathrm{RMS}}\frac{aV_{ce}^{\mathrm{SAT}}}{2}. \tag{21}$$

The first equation in (20) can also be written as

$$p_T^{\mathrm{LF}}(t) = \alpha_1 \sin\left(\frac{2\pi}{T}t - \varphi\right) + \frac{\alpha_2}{2}\cos(\varphi) - \frac{\alpha_2}{2}\cos\left(\frac{4\pi}{T}t - \varphi\right). \tag{22}$$

Starting from (22), a pessimistic approximation for $\hat{P}_T^{\mathrm{LF}}$ is given by the following equation

$$\hat{P}_T^{\mathrm{LF}} \cong \alpha_1 + \frac{\alpha_2}{2}[1 + \cos(\varphi)]. \tag{23}$$

In fact, (23) gives an exact value for $\hat{P}_T^{\mathrm{LF}}$ when $\varphi = 0$, while in all other realistic cases it only slightly overestimates the peak of the power losses. On this basis, the following equation is easily obtained

$$\hat{P}_T^{\mathrm{LF}} = \sqrt{2}\left(f_C V_{\mathrm{IN}}\tau_{\mathrm{EQ}} + V_{ce}^{\mathrm{SAT}}\left\{\frac{1}{2} + \frac{a}{4}[1 + \cos(\varphi)]\right\}\right)I_{\mathrm{RMS}}. \tag{24}$$

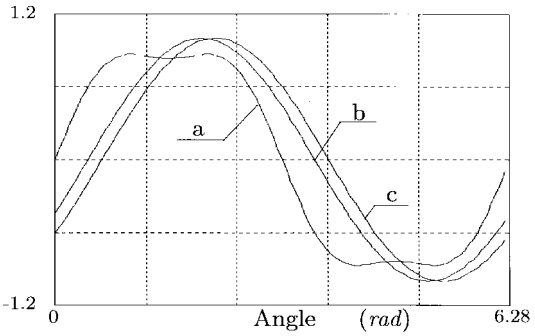

Fig. 9. Waveform (a) represents the shape of the function $\sin[(2\pi/T)t] + \frac{1}{6}\sin[(6\pi/T)t]$ while waveforms (b) and (c) represent the shape of $i_T^{\mathrm{LF}}(t)$. Waveform (b) refers to $\cos(\varphi) = 0.9$ while waveform (c) refers to $\cos(\varphi) = 0.8$.

When a PWM modulation with third harmonic predistortion is considered, the instantaneous duty-cycle becomes

$$\rho(t) = \frac{1}{2} + \frac{a}{2}\left[\sin\left(\frac{2\pi}{T}t\right) + \frac{1}{6}\sin\left(\frac{6\pi}{T}t\right)\right]. \tag{25}$$

As it is well-known, in a three-phase converter the phase-to-phase voltage is still sinusoidal when the third harmonic predistortion is introduced on each phase; thus, also the output current is still sinusoidal and can again be expressed by means of (19). In such conditions, the power peak value can be more accurately estimated since, as shown in Fig. 9, $\rho(t)$ is particularly flat near its maximum. Thus, any reasonably limited variation of $\cos(\varphi)$ introduces only small variations in the peak value of the product $\rho(t)i(t)$. For this reason, the maximum value of that product can be evaluated as

$$\max_t\{\rho(t)i(t)\} \cong \max_t\{\rho(t)\}\max_t\{i(t)\}, \tag{26}$$

where

$$\max_t\{\rho(t)\} = \frac{1}{2} + \frac{a}{2}\,\frac{\sqrt{3}}{2}, \max_t\{i(t)\} = \sqrt{2}I_{\mathrm{RMS}}. \tag{27}$$

Also for the third harmonic predistortion, the power peak is given by the maximum of (16). Bearing in mind (26), $\hat{P}_T^{\mathrm{LF}}$ can be written as

$$\hat{P}_T^{\mathrm{LF}} = \sqrt{2}\left\{f_C V_{\mathrm{IN}}\tau_{\mathrm{EQ}} + V_{ce}^{\mathrm{SAT}}\left[\frac{1}{2} + \frac{a}{2}\,\frac{\sqrt{3}}{2}\right]\right\}I_{\mathrm{RMS}}. \tag{28}$$

Comparison of (24) and (28) leads to the conclusion that for typical values of $\cos(\varphi)$ (i.e., $\cos(\varphi) \in [0.8, 1]$), the third harmonic distortion gives a power peak dissipation slightly

lower than the one that can be obtained with a classical purely sinusoidal modulation.

Also P_{T0} must be evaluated by using (16). To highlight a peculiar characteristic of $P_{T0}, \rho(t)$ is represented with a Fourier series, so that (16) becomes

$$p_T^{\mathrm{LF}}(t) = \begin{cases} \alpha_1 + \alpha_2 \displaystyle\sum_{j=1}^{\infty} c_j \sin\left(j\frac{2\pi}{T}t\right) \sin\left(\frac{2\pi}{T}t - \varphi\right), \\ \qquad \text{when } \sin\left(\frac{2\pi}{T}t - \varphi\right) > 0 \\ 0, \qquad \text{when } \sin\left(\frac{2\pi}{T}t - \varphi\right) \le 0 \end{cases} \tag{29}$$

with α_1 and α_2 defined by (21).

By applying (5) to (29), the following expression is obtained

$$P_{T0} = \frac{\alpha_1}{\pi} + \frac{\alpha_2}{2T} \sum_{j=1}^{\infty} c_j \int_{\varphi}^{T/2+\varphi} \cos\left[\frac{2\pi}{T}(j-1)t + \varphi\right] - \cos\left[\frac{2\pi}{T}(j+1)t - \varphi\right] dt \tag{30}$$

which gives an interesting result. In fact, when j is odd and different from 1, the integral is equal to zero. Thus, all modulation laws that are only composed by odd harmonics, have the same mean power losses. For both laws considered in this work we have

$$P_{T0} = \frac{\alpha_1}{\pi} + \frac{\alpha_2}{4}\cos(\varphi) \tag{31}$$

or, equivalently,

$$P_{T0} = \sqrt{2}\left\{\frac{f_C V_{\mathrm{IN}} \tau_{\mathrm{EQ}}}{\pi} + V_{ce}^{\mathrm{SAT}}\left[\frac{1}{2\pi} + \frac{a}{8}\cos(\varphi)\right]\right\} I_{\mathrm{RMS}}. \tag{32}$$

VI. Thermal Rating for a PWM-Controlled DC/AC Converter

The analytical dynamic thermal model proposed in this paper can be conveniently used in the design of PWM-controlled DC/AC power converters. In fact, when a simplified thermal analysis approach is available, the upper limits on operating conditions (i.e., load current, converter frequency, etc.) can be directly expressed in terms of a given upper limit on the junction temperature.

In such a context, different design scenarios can be outlined. In the following, two possible ways of using the expressions proposed in this work are introduced, but other applications could also be imagined. In the first situation, for a given electron device (e.g., chosen for the actual maximum operating peak current) and given converter operating conditions, the thermal analysis is used to define an upper limit for the case temperature (i.e., the minimum required heatsink efficiency). In the second example, for a given maximum case temperature and given converter operating conditions, a criterion for choosing the minimum allowable "size" of the electron devices is indirectly determined by defining an upper limit on R_{jc}. In all the examples, the case temperature θ_C is supposed to be time-invariant (because of the large thermal time constant of the case-sink system) and must not exceed an upper limit θ_C^{LIM}.

A. Determination of the Maximum Allowable Case Temperature θ_C^{LIM}

When the operating conditions are all known for a given electron device, the peak junction-to-case thermal drop Ψ can easily be computed by means of (4). In such conditions, the maximum allowable case temperature can be directly determined as

$$\theta_C^{\mathrm{LIM}} = \theta_j^{\mathrm{LIM}} - \Psi. \tag{33}$$

Equation (33) indirectly provides a constraint for heatsink system design. Such a limit can be satisfied by considering the maximum ambient temperature and the average power dissipation for each device [e.g., computed according to (32)] sharing the same heatsink. If the resulting constraint on the heatsink efficiency appears to be technically or economically too hard (i.e., the required θ_C^{LIM} is too low for the given ambient temperature range) another device, of a larger size and, consequently, with a lower R_{jc}, must be chosen. Conversely, if the resulting constraint on heatsink efficiency appears to be relatively weak, this might suggest that a smaller, cheaper device could be chosen. In both cases, the following procedure can be used for a more correct device choice.

B. Determining the Minimum Device Size by Computing R_{jc}^{LIM}

In this case, a family of technologically similar devices of different sizes is considered as possible candidates for the converter design. Normally, devices of different sizes but belonging to the same family have quite similar electrical parameters (V_{ce}^{SAT} and τ_{EQ}), similar thermal time-constant τ, but quite different values of R_{jc}^{LIM}, that are inversely proportional to the chip size (and also approximately to its cost). Thus, for a given family, all the device parameters are known, apart from R_{jc}^{LIM}. In such conditions, if a given suitable value of θ_C^{LIM} is chosen (actually, this is an *a priori* feasibility constraint for the heatsink system), the manufacturer's limit on junction temperature θ_j^{LIM} directly provides, by means of (7), an upper limit on the device thermal resistance. On this basis, the choice of the minimum-sized transistor can be correctly made; then, a more precise verification of the safe thermal operating condition can be performed by introducing the parameters of the device chosen into (7).

VII. Simulation of the Thermal Behavior of a Commercial IGBT

The analytical approach to thermal analysis described above involves several, mildly pessimistic approximations (e.g., $p_T^{\mathrm{LF}}(t)$ instead of $p(t), \Psi$ instead of the actual $\Delta\hat{\theta}$, conduction and switching losses linearly dependent on $i(t)$ and independent from temperature, etc.). In order to verify that such approximations do not lead to an excessively pessimistic estimate of $\Delta\hat{\theta}$, the thermal model equations (3) have been numerically solved by directly considering the actual voltage and current waveforms in an inverter driving an asynchronous motor according to a field-oriented control algorithm. The numerical analysis was carried out by using the MICOSS simulator [14]. Owing to the complexity and the relatively

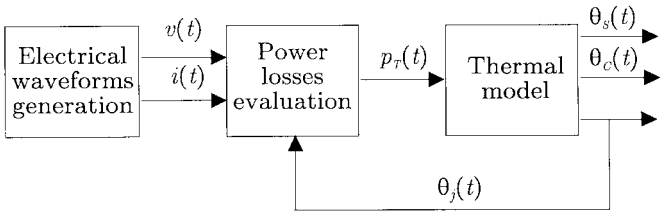

Fig. 10. Electro-thermal simulation scheme.

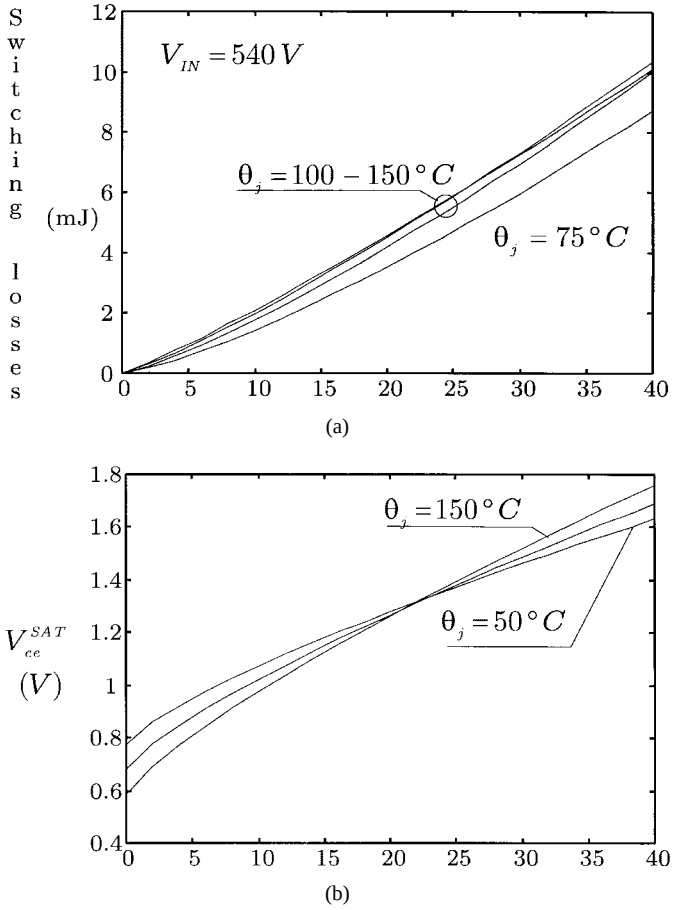

Fig. 11. Values of $V_{ce}^{\rm SAT}$ and $E_{\rm TOT} = E_{\rm on} + E_{\rm off}$ versus load current and junction temperature.

high computational time of a fully coupled electro-thermal simulation of a PWM-controlled converter with nonideal electron device models, a simplified partially decoupled approach, similar to that used in [9], has been adopted. The simulation scheme is shown in Fig. 10. First a numerical simulation of the PWM converter (including control algorithm and load motor model) is carried out by considering ideal switches. On this basis, the time varying electrical stresses (i.e., switched currents) are determined. Conduction and switching losses have been evaluated, for each single conduction interval and switching event, according to the mathematical models proposed in [4]. These analytical expressions enable $E_{\rm on}, E_{\rm off}$, and $V_{ce}^{\rm SAT}$ to be computed as functions of the transistor electro-thermal stresses (i.e.,$V_{\rm IN}, i(t)$, and θ_j). In particular, Fig. 11 shows the corresponding current and temperature dependent values of $V_{ce}^{\rm SAT}$ and $E_{\rm TOT} = E_{\rm on} + E_{\rm off}$, used in our simulation, for

TABLE I
PARAMETERS OF AN IGBT IRGPC50F (FROM DATA SHEETS)

τ_{EQ}	$462.96{*}10^{-9}$ s
τ	0.04 s
f_θ	3.98 Hz
V_{ce}^{SAT}	1.8 V
R_{jc}	0.64 °C/W

TABLE II
LOAD AND CONVERTER CHARACTERISTICS

	$T = 155$ ms; $f = 6.5$ Hz	$T = 27$ ms; $f = 37.0$ Hz
I_{RMS}	25.08 A	26.91 A
a	0.1875	0.8475
$\cos(\varphi)$	0.9268	0.9397
V_{IN}	540 V	540 V
f_C	10 KHz	10 KHz

TABLE III
ESTIMATION OF THE MEAN AND PEAK VALUES OF THE POWER LOSSES AND OF THE MAXIMUM JUNCTION-TO-CASE THERMAL DROP FOR THE CONSIDERED IGBT

	$T = 155$ ms; $f = 6.5$ Hz		$T = 27$ ms; $f = 37.0$ Hz	
	Sinusoidal	Third harm.	Sinusoidal	Third harm.
P_{T0}	39.77 W		48.01 W	
$\hat{P}_T^{LF}$	126.36 W	125.78 W	157.54 W	154.53 W
Ψ	58.19 °C	58.06 °C	38.19 °C	38.12 °C

the IGBT IRGPC50F. It can be noted that switching energies are almost linearly current dependent and mildly temperature dependent. Moreover, $V_{ce}^{\rm SAT}$ shows only a mild dependence on both current and temperature.

The model coefficients given in [4] are obtained by direct measurements on commercial transistors, thus assuring good agreement with actual devices. By using this model, the instantaneous power losses $p_T(t)$, to be used as the forcing term in the numerical solution of (3), are easily obtained. The thermal feedback (see θ_j in Fig. 10) is needed since loss models are temperature dependent.

The IGBT parameters, obtained from the data sheet of the device used, are summarized in Table I.

Two situations have been considered as particularly interesting, practical cases. In the first, the motor rotates very slowly, so that the output frequency of the power converter (6.5 Hz) is close to the thermal cutoff frequency (3.98 Hz). In the second, the velocity is increased until the output frequency reaches 37 Hz, which is much higher than the thermal cut-off frequency. The load and the converter characteristics, for the two operating conditions considered, are shown in Table II.

The values of $P_{T0}, \hat{P}_T^{\rm LF}$, and Ψ, evaluated according to (4), (24), (28), and (32), are given in Table III. Both a sinusoidal modulation and a sinusoidal modulation with third harmonic distortion have been considered. As predicted by our analysis, the third harmonic distortion produces a smaller Ψ than a purely sinusoidal modulation.

In Fig. 12, simulated results are compared with those given in Table III. Both figures refer to a purely sinusoidal modulation. Acceptable agreement can be found between analytically estimated values and numerically computed ones (by using measurement-based loss models). As expected, the estimated

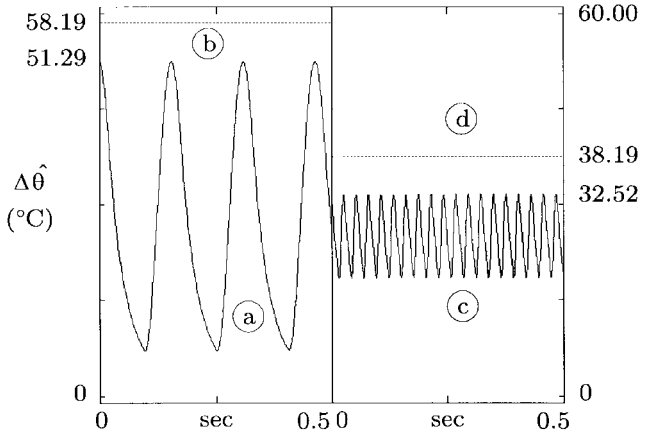

Fig. 12. Junction to case thermal drop. Solid line (a) refers to simulation made using accurate loss models [4], while dashed line (b) represents the peak value estimated by using (4). The first converter simulation corresponds to an asynchronous motor drive with output frequency $f = 6.5$ Hz. The corresponding curves (c) and (d), in the second graph, have been obtained in the same way but with $f = 37$ Hz.

thermal drop only slightly overestimates the real case-to-junction temperature drop. In the first graph shown in Fig. 12, a converter output frequency equal to 6.5 Hz is considered. This is the worst condition for the estimation procedure proposed in this work since the output frequency is close to the thermal cut-off frequency. In spite of this, not a very large percentage error, equal to 13.4%, has been found. In the situation shown in the second graph in Fig. 12, the output frequency is much higher and the percentage error is equal to 17.4%.

VIII. Conclusion

The proposed thermal analysis approach can be used to estimate, with acceptable accuracy, the junction peak temperature of an IGBT device. In spite of the approximations introduced to obtain an analytical solution, reasonable agreement with the results of accurate simulations, carried out by using measurement-based loss models, has been found. The analytical approach for estimating the peak junction temperature can be easily applied on the sole basis of device parameters and graphs normally available on manufacturers data-sheets. On this basis, thermally safe operating conditions can be easily verified even in the more difficult, yet common case, of PWM DC/AC converters with low output frequencies. The same approach can also be used for correct transistor/heatsink choice in converter design; moreover, it also allows for easy comparison of different PWM modulation strategies in terms of thermal stresses on power devices.

Appendix A

To find an upper bound Ψ on the peak temperature drop $\Delta\hat{\theta}$, the actual shape of the power losses is replaced by a simpler worst-case one that has the same P_{T0} and $\hat{P}_T^{\mathrm{LF}}$. By considering the convolution defined in (3), it can be immediately observed that a slightly pessimistic approximation is obtained if power losses are concentrated in a single rectangular pulse whose amplitude is equal to $\hat{P}_T^{\mathrm{LF}}$ (see Fig. 13) and whose width

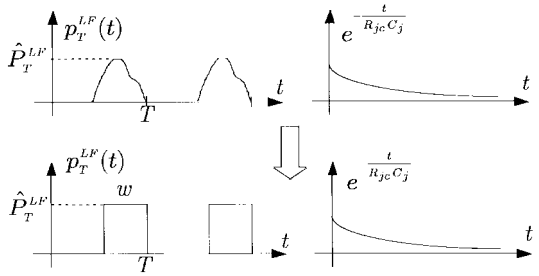

Fig. 13. Shape of the power losses and its approximation by means of a rectangular pulse.

necessarily corresponds to the given value of P_{T0}. This condition is clearly satisfied by a pulse duration w given by

$$w = \frac{P_{T0}T}{\hat{P}_T^{\mathrm{LF}}}. \tag{34}$$

The maximum of $\Delta\theta(t)$ is obviously reached at the end of the rectangular pulse. Thus, it is possible to get a suitable value for Ψ by adopting this shape for $p_T^{\mathrm{LF}}(t)$ and by solving (3) for $\Delta\theta(t)$. The required upper bound on the peak temperature Ψ is given by

$$\Delta\hat{\theta} \le \Psi = R_{jc}\hat{P}_T^{\mathrm{LF}}\frac{1-e^{-(w/\tau)}}{1-e^{-(T/\tau)}}. \tag{35}$$

Equation (4) is finally obtained by substituting (34) into (35).

Appendix B

If a sinusoidal modulation is assumed, the output voltage for the three phases of the converter can be expressed as

$$v_k(t) = V_{\mathrm{IN}}\left[\frac{1}{2} + \frac{a}{2}\sin\left(\frac{2\pi}{T}t + k\frac{2}{3}\pi\right)\right], \qquad k = 0, 1, 2; \tag{36}$$

thus, the neutral voltage is given by

$$V_N = \frac{v_0 + v_1 + v_2}{3} = \frac{V_{\mathrm{IN}}}{2}. \tag{37}$$

The phase-to-neutral voltage for a linear symmetric load can be easily evaluated. For example, for the phase 0, it is given by

$$v(t) = v_0(t) - V_N = V_{\mathrm{IN}}\left[\frac{a}{2}\sin\left(\frac{2\pi}{T}t\right)\right]. \tag{38}$$

Equation (38) shows that the phase-to-neutral peak voltage $\hat{V}$ is equal to $(V_{\mathrm{IN}}a)/2$. Because $V_{\mathrm{RMS}} = \hat{V}/\sqrt{2}$, a few algebraic manipulations lead to (18).

For a sinusoidal modulation with third harmonic distortion, the neutral voltage is time-dependent

$$v_N(t) = V_{\mathrm{IN}}\left[\frac{1}{2} + \frac{a}{12}\sin\left(\frac{6\pi}{T}t\right)\right]. \tag{39}$$

The difference between the neutral and the output voltages leads to (38), so that the modulation index a can be expressed again by means of (18).

REFERENCES

[1] J. W. Kolar, H. Ertl, and F. C. Zach, "Calculation of the passive and active component stress of three-phase PWM converter systems with high pulse rate," in *Proc. 3rd Europ. Conf. Power Electron. Appl.*, Aachen, Germany, Oct. 9–12, 1989, vol. 3, pp. 1303–1311.

[2] C. H. Schaeffer, J. P. Ferrieux, M. L. Locatelli, S. H. Gamal, and S. Volut, "Investigation on high-temperature operation for IGBT components," in *Proc. 4th Europ. Conf. Power Electr. Appl. (EPE'91)*, Firenze, Italy, Sept. 3–6, 1991, vol. 2, pp. 484–490.

[3] A. Boglietti, P. Ferraris, and F. Profumo, "Losses evaluation in high-power devices PWM inverter motor drives," in *Proc. 4th Europ. Conf. Power Electr. Appl. (EPE'91)*, Firenze, Italy, Sept. 3–6, 1991, pp. 386–392.

[4] S. Clemente, "Application characterization of IGBT's," *Int. Rectifier AN-990*, El Segundo, CA, 1992.

[5] _____, "A simple tool for the selection of IGBT's for motor drives and UPS," in *IEEE Applied Power Electronics Conf. (APEC95)*, Dallas, TX, Mar. 5–9, 1991, pp. 755–764.

[6] A. K. S. Bhat and M. M. Swamy, "Loss calculations in transistorized parallel resonant converters operating above resonance," *IEEE Trans. Power Electron.*, vol. 4, no. 4, Oct. 1989.

[7] J. H. Rockot, "Losses in high-power bipolar transistors," *IEEE Trans. Power Electr.*, vol. PE-2, no. 1, Jan. 1987.

[8] F. Blaabjerg, U. Jaeger, S. Munk-Nielsen, and J. K. Pedersen, "Power losses in PWM-VSI inverter using NPT or PT IGBT devices," in *PESC94*, Taipei, Taiwan, R.O.C., June 1994, pp. 434–441.

[9] S. Konrad and K. Anger, "Electro–thermal model for simulating chip temperatures in PWM inverters," in *Power Conversion and Intelligent Motion Conf. (PCIM95)*, Nuremberg, Germany, June 1995, pp. 219–228.

[10] A. Kurnia, H. Cherradi, and D. M. Divan, "Impact of IGBT behavior on design optimization of soft switching inverter topologies," in *IEEE Trans. Ind. Applicat.*, vol. 31, pp. 280–286, Mar./Apr. 1995.

[11] J. W. Kolar, H. Ertl, and F. C. Zach, "A comprehensive design approach for a three-phase high-frequency single-switch discontinuous-mode boost power factor corrector based on analytically derived normalized converter component ratings," *IEEE Trans. Ind. Applicat.*, vol. 31, pp. 569–582, May/June 1995.

[12] K. Wang, F. C. Lee, G. Hua, and D. Borojevic, "A comparative study of switching losses of IGBT's under hard-switching, zero-voltage-switching and zero-current-switching," in *PESC94*, Taipei, Taiwan, R.O.C., June 1994, pp. 1196–1204.

[13] R. Redl and L. Balogh, "RMS, DC, peak and high-frequency power-factor correctors with capacitive energy storage," in *Proc. 7th Appl. Power Electron. Conf.*, Boston, MA, Feb. 23–27, 1992, pp. 533–540.

[14] C. Bonivento, A. Tonielli, and R. Zanasi, *Simulazione di sistemi dinamici con programma MICOSS*, (in Italian). Bologna, Italy: Pitagora Editrice, 1990.

Fabio Filicori was born in Imola, Italy on January 8, 1949. In 1974 he graduated in electronic engineering at the University of Bologna, Italy, where, in the same year, he started his academic career at the Istituto di Elettronica as a Research Assistant in Radio Electronics.

From 1980 to 1989, he was an Associate Professor of Applied Electronics at the University of Bologna, Italy. In 1990, he became a Full Professor of Applied Electronics at the University of Perugia, Italy. The following year he moved to the University of Ferrara, where he was a Full Professor from 1991 to 1994. In November 1994 he joined the Dipartimento di Elettronica, Informatica e Sistemistica of the University of Bologna, Italy, as a Full Professor of Industrial Electronics. During his academic career he has taught courses on applied electronics, industrial electronics, and computer-aided design of electronic circuits. Since 1991, he has been President of the Academic Committee for the degree course in electronic engineering at the University of Ferrara. He is also the Coordinator of the Academic Committee for the P.D.H. course in electronic and computer science engineering at the University of Bologna. His research activity has been mainly devoted to the modeling of electron devices and electronic circuit design, with special emphasis on computer-oriented numerical approaches. In particular, he has been working in the areas of nonlinear circuit analysis and design, electron device modeling, power electronics, and digital measurement instruments.

Corrado Guarino Lo Bianco was born in Sassari, Italy, on May 3, 1964. He graduated with honor in electronic engineering in 1989 from University of Bologna, Italy, and in 1994 he received the Ph.D. degree from the same university.

In 1997, he joined the Dipartimento di Ingegneria dell'Informazione of the University of Parma as an Associate Researcher. His research concerns the application of genetic and interval algorithms in the field of linear and nonlinear control, the study of the thermal behavior of power converters, and the development of algorithms for smooth trajectory generation for motion control. He is also interested in digital motor control with particular regard to modeling and controlling of variable reluctance motors and asynchronous motors.