

Digital Circuits in a Multi-Functional SAGFET MMIC Technology

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ABSTRACT

In this paper a possible implementation of digital circuits in a MMIC SAGFET/SAGHEMT technology is described. This technology has been developed at the Alenia Marconi Systems (AMS) and it is well suited for the integration of digital and microwave parts in the same GaAs substrate. A test circuit with FET's for DC/AC characterization, inverter chains, ring oscillators and frequency dividers has been designed and is now under fabrication at AMS. Since now only Depletion MESFET transistors were available. However, the technology is still growing and in the near future Enhancement and Depletion MESFET and HEMT transistors will allow the implementation of E/D logic circuits.

INTRODUCTION

The integration of both digital and microwave circuits in the same substrate is an important and still not well addressed issue. The reduction of the overall weight and volume is mandatory especially for satellite equipments and portable apparatus. Therefore there is a need for the development of technologies which can support both operations in a multi-functional environment. Alenia Marconi Systems (AMS) developed recently a Self-Aligned FET (SAGFET/SAGHEMT) process for this purpose in the frame of the CNR MADESS-II project. The source and drain series resistances which affect the FET performance [1] are mostly reduced by the SAGFET/SAGHEMT technology. This leads to a large improvement in both cutoff frequency and switching speed for the microwave and for the digital part respectively.

The overall objective of the MADESS-II project is to develop an advanced technology for the fabrication of GaAs monolithic integrated circuits based on "self-aligned" transistors SAGFET and/or SAGHEMT and use this technology for the fabrication of high performance, low cost mono and multi-functional analog/digital integrated circuits. This work was focused on the development, modeling and design of the digital subsystems.

SELF-ALIGNED TECHNOLOGY DESCRIPTION

The main steps of the MESFET process are described in Fig. 1. The self-aligned ion implantation across the tungsten nitride (WN) layer delineates the source-gate-drain structure of the device. A gold deposition over the WN layer is etched by CF₄ RIE in order to define the Schottky contact. After the ohmic electrode fabrication a selective CF₄ plasma etch defines a T-gate structure. In Fig. 2 are depicted the main steps for the fabrication of the HEMT transistors. The devices are separated through protons implantation. The resulting high isolation is an important added value for mixed-signal environments like those of multi-functional circuits. The gate and contact self-aligned definition are obtained via a 0.5 μm gold shoulder as illustrated in the figure. A very low resistivity ohmic contact for drain and source is obtained through an alloying process at temperature lower than 600°C which

is the maximum temperature for the optimized metallic layer used in the Schottky contact. The main feature of such a contact is its capability to penetrate across the epitaxial layer and create a very good contact. Besides the gate and the ohmic contact another layer is available for the interconnections. Its ohmic resistance can be furtherly reduced with a thick gold layer growth over this metal.

DESIGN OF DIGITAL CIRCUITS

At the present stage of development only a Depletion MESFET is available in the AMS SAG-FET/SAGHEMT technology. The Depletion HEMT is now in its optimization phase while the Enhancement MESFET and HEMT are under development but not still available for the design purposes. This situation reduces the space of the solutions for digital circuits. Only classic Depletion-Mode logic circuits [2] can be implemented. Nevertheless this type of logic circuits has the interesting property of an inherent robustness to the variations of the process parameters which is useful in the early stage of development when test vehicles must be implemented. The Buffered FET Logic (BFL) has been chosen for the implementation of the logic gates. Depletion-Mode circuits require three power rails (V_{dd} , V_{ss} (negative) and gnd) instead of the two for Enhancement-Depletion circuits (V_{dd} , gnd). This is not a problem for MMIC because a negative power supply is common for the bias of the FET based amplifiers. As soon as the Enhancement transistors will be available other more advanced E/D structures will be conceived.

A MMIC for digital characterization has been laid-out. The layout consists of single FETs designed for the DC/AC characterization and some digital structures. The generated masks can be used for both the MESFET and the HEMT based process. The 12 FETs for the DC measurements have width in the range $5 \div 60 \mu\text{m}$. Those for AC characterization are 4 and have width in the range $25 \div 100 \mu\text{m}$. The drawn length is $0.5 \mu\text{m}$ but the effective length is reduced to about $0.25 \mu\text{m}$ through the process steps indicated in Fig. 1-2. The bigger size for the AC testable FETs avoids the inclusion of relatively large parasitics in the measurements. In addition, as we observed testing other commercial GaAs processes, the gate capacitance scales well with the MESFET size, better than static I_{ds} which is affected by a geometry-dependent behavior in the submicron domain. Therefore the AC data will be suitable also to model smaller transistors applying a scaling rule.

A simple digital library has been designed which consists of a BFL inverter (INV) and two BFL NOR gates with 2 and 3 inputs (NOR2 and NOR3) as illustrated in Fig. 3. A conservative approach based on the experience of design with other GaAs processes has been used for the sizing of the transistors and Schottky diodes. These cells have been used as instances for the design of an inverter chain (5 stages), a weakly loaded ring oscillator (7 stages, fan-out=2) and another ring oscillator driving a flip-flop frequency divider by 256 (8 stages). The layouts are reported in Fig. 4.

Each one of the 5 inverters connected in chain is provided with an output pad for the measurements of the propagation delays and for the analysis of the waveforms. The ring oscillator consists of NOR2 gates. One of the inputs is used as *enable* control signal. In order to reduce the load and to measure the intrinsic frequency of oscillation, the output is capacitively coupled to a high impedance Source-Follower. This amplifier provides the current to drive a high frequency probe. A 50Ω controlled impedance pad for the probe is used (see Fig. 4(b)). The MIM capacitor used for the AC coupling is formed by a reactive sputter deposition of Si_3N_4 sandwiched between ohmic contact layer and metal layer. An identical ring oscillator provides the input frequency to the divider each stage of which is a Toggle flip-flop. The transistor count for the divider is 344 and the active area (pads and oscillator excluded) is about 1.6 mm^2 . The lack of other levels of metalization, which is common in digital GaAs processes but, alas, unusual in MMIC, reduces the integration density and poses several constraints in the layout.

The DC and AC measurements of the single FETs will be used to tune the parameters of the Statz large signal model [3] which is universally used for time-domain circuit simulation. The model will be refined according to the delay and frequency measurements taken from the digital circuits. An extraction procedure for the Statz model parameters has been tested with another GaAs digital commercial process.

CONCLUSIONS

An implementation of digital circuits compatible with microwave parts in the same MMIC on a GaAs substrate is described in this paper. This possible cohabitation is interesting for the weight and volume reduction in satellite and portable electronic apparatus. The same Self-Aligned Depletion FET can be used for digital and microwave design. A SAGFET/SAGHEMT technology has been developed by the Alenia Marconi Systems (AMS) for the implementation of mono and multi-functional integrated circuits. A test circuit for the characterization of the FETs and of some BF-Logic cells has been designed and is now under fabrication at AMS.

ACKNOWLEDGMENTS

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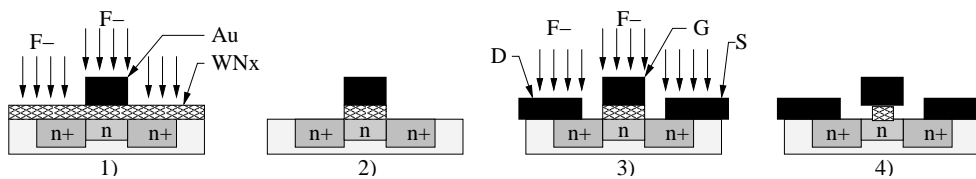


Figure 1: MESFET process: 1) Self align implantation across WN layer, gold structure define active channel; 2) Schottky contact definition by selective CF_4 RIE; 3) After ohmic electrode fabrication, T-gate electrode definition by selective CF_4 plasma etch; 4) SAGFET device

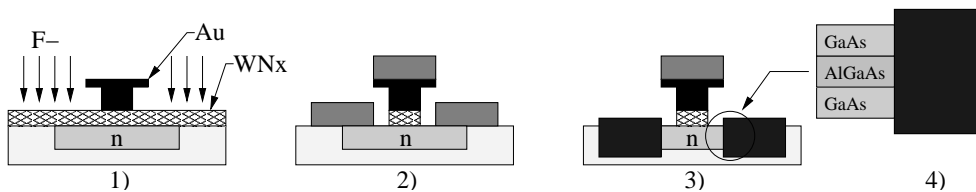


Figure 2: HEMT process: 1) Schottky contact definition by selective CF_4 plasma etch of the WN; 2) Self align ohmic electrode formation using the $0.5 \mu\text{m}$ shoulder of gold; 3) Ohmic contact alloying process at $T < 600^\circ\text{C}$; 4) Ohmic contact penetration across epitaxial heterostructure layer.

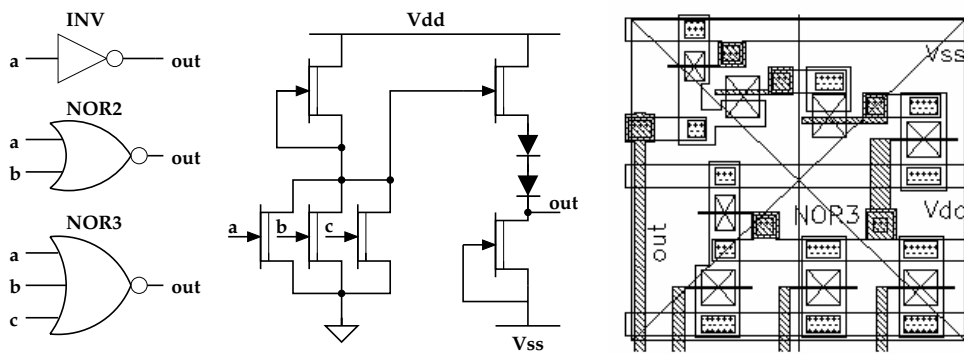


Figure 3: INV, NOR2 and NOR3 symbols; NOR3 schematic and layout. The inverter and the 2 input NOR schematic and layout are similar.

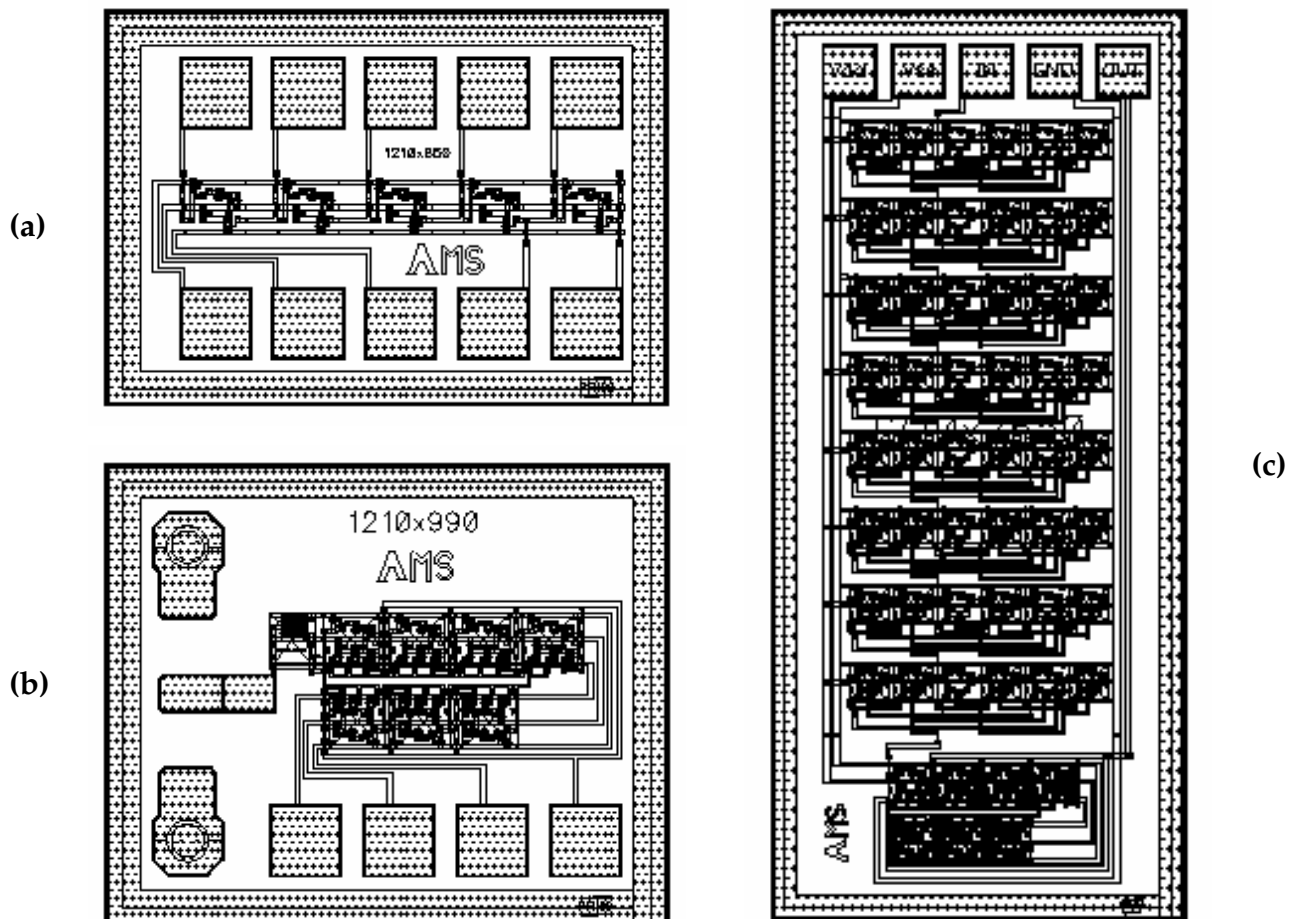


Figure 4: Layout of the 5 stage inverter chain (a), the 7 stage fanout=2 ring oscillator (b) and the flip-flop divider by 256 (c).