

SILICON TECHNOLOGIES FOR RF APPLICATIONS

Pietro Erratico

STMicroelectronics
Via Tolomeo, 1 - Cornaredo (Milan) - Italy
e-mail: pietro.erratico@st.com

ABSTRACT

The following paper would like to give an idea of the present status of silicon technologies used for the analog front-end of communication systems. The frequency spectrum of application is that of the mobile communications standards (up to few GigaHertz).

A short description of the available active devices (CMOS, SiGe BJT, DMOS) will be presented. In addition some information regarding the feasibility of good quality passive components (Inductors, Capacitors, Varactors, Resistors) will be given.

INTRODUCTION

In the last years we assisted to a continuous and regular improvement of the CMOS technologies, that is commonly known as Moore law.

This is normally evaluated in term of density improvement, i.e. every 18 months we see a doubling of the gate density or memory size in a given area. We can say that from 1988 to 2001 we passed from 1.2μ to 0.12μ , so we have probably gained a factor one hundred in density.

In 0.12μ technology the feasibility of $200\text{kgate}/\text{mm}^2$ or gigabit size memories has been demonstrated.

CMOS ACTIVE DEVICES

It is less common to consider how much this progress has affected the speed of transistors, apart maybe from what is emerging from Intel Family Speed that passed from about 50 MHz to 1 GHz clock in the same period of time.

That is obviously less dramatic due to the fact that supply voltage changed from 5 to 1 volt in the meanwhile. This is a necessity for the silicon dioxide nature per se, but it is also a must if we want to control the power dissipation of a multimillion gate device: indeed quite often we work at a voltage even lower than the maximum possible exactly for this reason.

Maybe a byproduct that nobody wanted, anyway we got a CMOS transistor with excellent speed performance: 50 Ghz ft, excellent Fmax mainly coming from a low resistance gate material, a low losses input circuit, good linearity, etc. (see Fig. 1).

All of that appears to be quite competitive with GaAs mesfet at least in the frequency range up to 3 Ghz that is the one currently considered for the majority of the portable and consumer applications. From the transistor point of view the only real limitation appear to be flicker noise that exist up to megahertz range, so the designer has to take care of any non linear effect that could convert it at higher frequencies: not dissimilar then several FET devices also in GaAs.

SILICON BIPOLAR DEVICES

Traditionally Bipolar transistor has been the race horse for silicon RF and, at the present time, it is still giving the most contribution to IC sales.

The major advantage is coming from a better gm/I performance, that could be very interesting for some low power application, and also from superior flicker noise performance.

SiGe technology is a very important plus, making available structures that could be considered similar to HBT in GaAs: their ft today is close to 100GHz with noise figure at 2 GHz better than 0.8dB (see Fig.2 and Table 1).

It is natural, at this point, to merge Bipolar and CMOS technologies to obtain what is usually called BiCMOS, today mainly a CMOS technology structure together with some extra modules (dedicated wells, SiGe devices, dedicated polysilicon steps for base and emitter, etc.) able to generate the required level of RF performance. On the other a lot of application will be served without this extra sophistication that increases cost in a significant way, at least in case of big chips, as a result of a significant logic section integration .

Substrate isolation is a key concern in this cases, for which dedicated CAD tools and flows have been developed and used.

DMOS DEVICES

A DMOS is a special MOS structures where the channel doping is not constant but has a special profile able to minimize transit time versus a given voltage ratings (see Fig. 3).

Several power amplifiers are looking for power capability in the range of 2/3 watts, hence a transistor breakdown requirement up to 12/15 volts even if supply voltage is only 5V.

The DMOS structure has what is needed to challenge also this kind of application, i.e. able to compete with GaAs MESFET mainly in term of cost and integration level .

That is particularly important for future cellular standard where the modulation scheme and the required PAE will ask for a power section far more complex than today constant envelope modulation amplifiers.

PASSIVE DEVICES

But RF is not only transistors: passive components will play a significant role as well, at least to get some low noise oscillator and some frequency selectivity/adaptation.

It is obvious that a silicon CMOS designer will and is even today paying his maximum effort to develop new architectures more suitable for the new economic paradigm, e.g. exchanging an external filter with some thousands transistors or a DSP functions, as it has been the case for any analog integration story in the past.

Nevertheless we need good inductors, capacitor, resistors.

Silicon is not used in the form of a semi-insulating substrate as GaAs is, so something has to be done to avoid inductance losses due to eddy current in the GigaHertz range. This suggest to avoid any highly doped substrate (as it is for digital EPI wafers). Sophisticated structures have been considered and proven, but may be not needed if a quality factor of about 10 is the objective.

Self resonance and capacitive losses can be cured with layout techniques to a reasonable extent .

The advent of copper metallurgy, mainly introduced for high speed logic, will reduce the ohmic losses to a big extent, in fact they still are the major limitation up to 1 GHz at least.

For capacitors, double poly structure borrowed for classical SC application could be acceptable, but Metal-Insulator-Metal structures with $T_{ox} \sim 30\text{nm}$ can guarantee better Q in the GigaHertz range.

Resistors are usually available as salicided poly even if dedicated thin film layers are by sure possible if better resistance control is requested, e.g. 50 Ohm terminations. All of that could be configured also as micro strip line structures if needed.

Varicap are possible in the classical junction capacitor form or even in various MOS configuration, able to guarantee up to a factor two of capacitance variation under 3 volt operations.

CONCLUSIONS

The mobility of GaAs is a fact that cannot be denied

Anyway the shrinkage path is bringing CMOS technologies to reach quite relevant performance in term of transistor basic parameters. On top of that , if we want to get real single chip integration of signal processing and RF front end, what we commonly define SOC, CMOS appears to be the only technology that can do it in industrial and efficient terms.

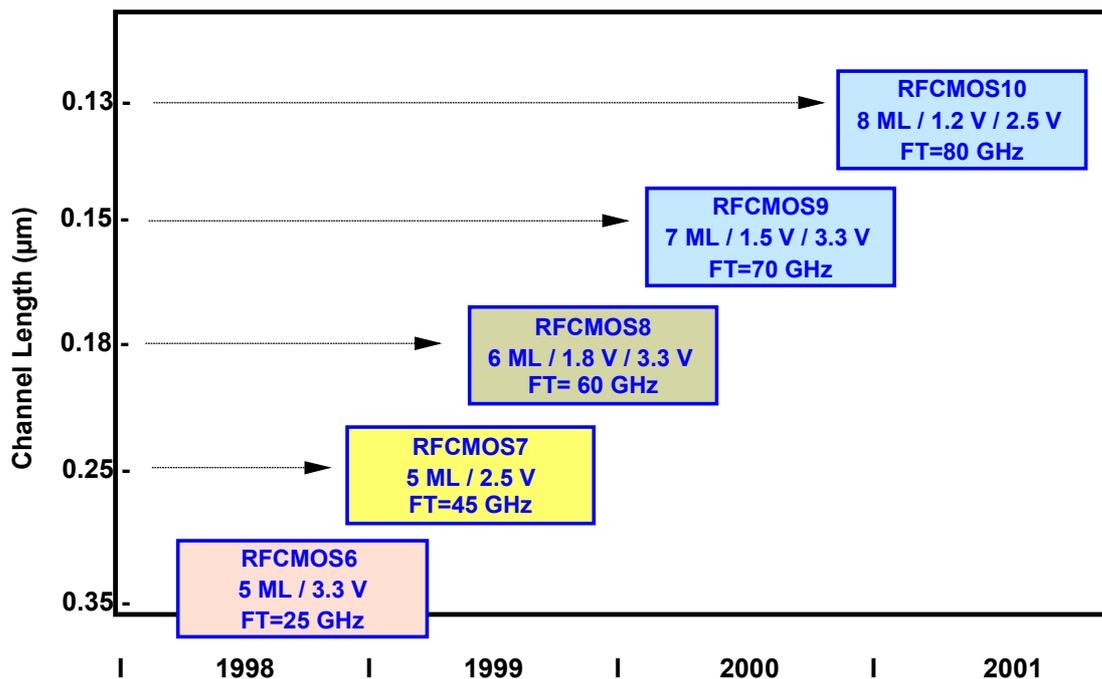


Fig. 1 STMicroelectronics Road Map for CMOS-RF Technologies

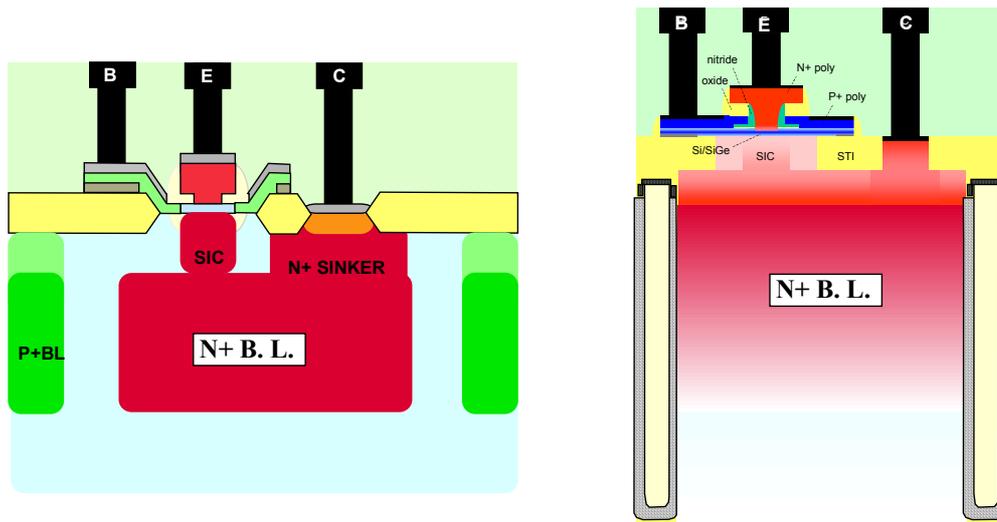


Fig. 2 SiGe HBT Transistors: Deep Trench Poly-Oxide Isolation (right)

	ST-BiCMOS6G	ST-BiCMOS7G
F _t (GHz)	45	70
F _{MAX} (GHz)	60	90
Self-Alignment	NO	YES
Isolation	LOCOS	S + D-Trench
CMOS	0.35μm	0.25μm

Table 1. STMicroelectronics SiGe HBT (Left: available, Right: Under Development)

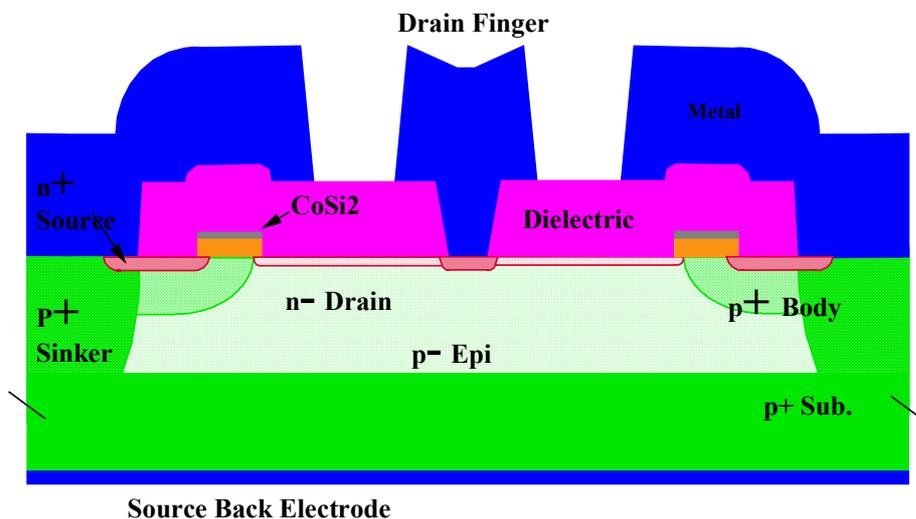


Fig. 3 Lateral DMOS Structure