

DESIGN OPTIMISATION OF ULTRA-SHORT GATE HEMTs USING MONTE CARLO SIMULATION

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ABSTRACT

By using a Monte Carlo simulator the static and dynamic characteristics of a 50 nm gate AlInAs/GaInAs δ -doped HEMTs are investigated. The Monte Carlo model includes some important effects that are indispensable when trying to reproduce the real behaviour of the devices, such as degeneracy, presence of surface charges, T-shape of the gate, presence of dielectrics and contact resistances. Among the large quantity of design parameters that enter into the fabrication of the devices, we have studied the influence on their performance of two factors: the doping level of the δ -doped layer and the length of the recess. We will show that the first one has a very important effect on the cutoff frequency and other important figures of merit of the transistor, and its value has to be carefully chosen. Conversely, we have also checked that the influence of the recess length is quite slight.

INTRODUCTION

The classical modelling of electronic devices meets important difficulties when dealing with advanced structures, like modern MESFETs and HEMTs, mainly due to their small size. The short dimensions of these devices lead to the appearance of very high electric fields inside them, and, consequently, the existence of hot carriers and velocity overshoot is common in submicrometer recessed gate MESFETs and HEMTs (1). Therefore, simple drift-diffusion or hydrodynamic modelling can not well reproduce the electron dynamics inside such short devices, and the Monte Carlo technique appears as the only possible choice (2). Moreover, in the case of heterojunction devices, the electron confinement can also give rise to quantum effects such as degeneracy, energy quantization in the channel and tunneling effect from the channel to the gate. If a correct description were required it would be necessary to self-consistently solve Poisson and Schrödinger equations, which, for the moment, is an unaffordable task in terms of computation time for a dynamic simulation.

In order to overcome these difficulties, we will make use of a semi-classical Monte Carlo model that locally takes into account the effect of the degeneracy by using the rejection technique (3). The rest of quantum effects are not considered in order to keep the calculation time at an acceptable level. The validity of this approach has been checked in previous works by means of the comparison with experimental results of static characteristics, small signal behavior and noise performance of a 0.1 μm gate HEMT (InP based) (4), (5). Using this Monte Carlo simulator as analysing tool, we will present a microscopic investigation of a 50 nm gate δ -doped AlInAs/GaInAs HEMT.

There are a lot of technological parameters (both geometrical and electrical) that can be modified to optimise the design of HEMTs: the composition of the different materials, the width of the device, the length, position, and depth of the recess, the thickness and doping of the different layers, etc. Historically, these

parameters have been optimised by classical simulation techniques or, when simulations are not physically applicable (for example, working with submicrometer gates), by the expensive ‘test and error’ procedures. With the use of computer simulation, the design optimisation can be made in a short time and with no waste of money. Therefore, extending the application domain of simulation tools is the best way of improving the design optimisation process, and Monte Carlo simulation plays an important role for the success of this task.

In next section we will try to optimise the value of two of the design parameters: the doping level of the δ -doped layer and the length of the recess. For this sake, simulations with different values of these parameters (always inside of the technological possibilities) will be performed, and their influence on the static and dynamic characteristics of the 50 nm gate HEMT will be analysed.

RESULTS

Our Monte Carlo model gives a correct estimation of the static characteristics, small signal behavior and noise performance in the case of a 0.1 μm gate HEMT (4), (5) but, when reducing the gate length up to 50 nm, Monte Carlo simulation has not been checked yet. Indeed, when trying to reduce the gate length, it is convenient to keep constant the aspect ratio (gate length over gate-to-channel distance) to avoid important short channel effects. Therefore, the layer structure must be changed with respect to that of the 0.1 μm gate HEMT; the distance between the gate and the channel (the joined thickness of the Schottky layer, δ -doped layer and spacer) must be reduced. The reduction of the gate-to-channel distance can lead to the appearance of a gate leakage current due to the tunneling of electrons from the channel to the gate, thus degrading the device performance. To minimise this effect, the lower limit for this distance is approximately 100 Å. Tunneling is not considered in the simulation and it can only be detected by means of the experimental measurement of the gate leakage current, which will be used to check the results of the model. Moreover, in the scaling down process, the value of the δ -doped layer doping is a key parameter, since it must be sufficiently low to avoid conduction through it, but high enough to fill up the channel. The charge of the δ -doped layer must also be able to screen the influence of the surface charge placed on the recess, thus avoiding the depletion of the channel, effect which depends also on the gate-to-channel distance. The result of the addition of these effects can only be taken into account through the simulation of the characteristics of the transistor when using different values of the δ -doping. In the following we present the results of this analysis.

We have performed simulations of the 50 nm gate HEMT (whose geometry is shown in Fig. 1) with three values for the δ -doping: 5, 6 and $7 \times 10^{12} \text{ cm}^{-2}$. In Fig 2 we show the drain current and the transconductance, g_m , obtained in these simulations together with the results of the 0.1 μm HEMT previously studied (4), (5). The lowest δ -doping ($5 \times 10^{12} \text{ cm}^{-2}$) is the same as that used in the fabrication of the 0.1 μm gate HEMT. As observed in Fig. 2, both the current and the transconductance decrease when the gate length is reduced from 100 to 50 nm, although an increase was expected. The cause for this degradation of the transport properties is the depletion of the channel provoked by the surface charges lying in the bottom of the recess, whose effect on the potential distribution reaches the channel due to the reduction of the gate-to-channel distance in the 50 nm gate HEMT. To solve this problem the value of the δ -doping must be raised. In Fig. 2 it is observed that the performance of the device is largely improved when the δ -doping is increased; the intrinsic transconductance reaches 1500 mS/mm for $6 \times 10^{12} \text{ cm}^{-2}$ and 1700 mS/mm for $7 \times 10^{12} \text{ cm}^{-2}$.

Nevertheless, the δ -doping cannot be increased indefinitely since it degrades the threshold voltage, V_T (in Fig. 2 it is observed that V_T changes from -0.1V for $5 \times 10^{12} \text{ cm}^{-2}$ to -0.25V for $6 \times 10^{12} \text{ cm}^{-2}$ and to -0.4V for $7 \times 10^{12} \text{ cm}^{-2}$). Also, the increase of the δ -doping can lead to conduction through the δ -doped layer (parasitic channel), effect that degrades the performance of the device.

Once the static characteristics of the devices are calculated we can analyse their dynamic response. The small signal equivalent circuit of the HEMTs has been calculated taking as a basis the Y parameters, determined by using the classical MC technique (6). One of the most important figures of merit of the transistors, the intrinsic cutoff frequency, $f_c = g_m / 2\pi C_{gs}$, is presented in Fig. 3. Here it is noticed how f_c is improved with the higher the δ -doping due to the increase of the transconductance.

The results of the simulations made in HEMTs with a shorter recess (20 nm instead of 100 nm at each side of the gate) are also plotted in Fig. 3. Their static characteristics (drain current and transconductance) are practically the same as those shown in Fig. 2 since the width of the channel (parameter that controls the static drain current) does not depend on the recess length. However, some differences appear when dealing with the dynamic behavior: the gate-source capacitance (that enters in the definition of f_c) increases slightly when increasing the recess length. That is why in Fig. 3 the maximum cutoff frequencies of the HEMTs with the shorter recess are higher than those of the devices with the longer one.

The recess length has also some influence on the electric field profile inside the devices. If it is enlarged, the high fields appearing between the gate and the drain can be somewhat reduced, thus attenuating the effect of impact ionisation. In our case the upper technological limit for the length of the recess is the value initially used (100 nm), which corresponds to the optimal situation in terms of reduction of impact ionisation. However, when looking at the maximum kinetic energy of electrons, there is only a difference of a few hundredths of eV between the devices with long (100 nm) and short recess (20 nm, also the lower technological limit). Therefore, in our case, the reduction of the recess improves the characteristics of the devices without increasing significantly impact ionisation.

Taking into account that the cutoff frequency is not much improved when passing from 6×10^{12} to 7×10^{12} cm^{-2} , the optimal value for the δ -doping (for the chosen thickness of the Schottky layer) depends on the requirements for the threshold voltage. If a V_T of -0.4V (like in the $0.1 \mu\text{m}$ HEMT) is acceptable, a value of 7×10^{12} cm^{-2} can be used. In the case that a higher V_T is needed the δ -doping must be decreased to 6×10^{12} cm^{-2} , which does not degrade substantially the device characteristics.

Finally, we remark that the data provided by the simulation (layer thickness, δ -doping and recess length) will be used in the fabrication process of 'optimised' 50 nm gate real HEMTs.

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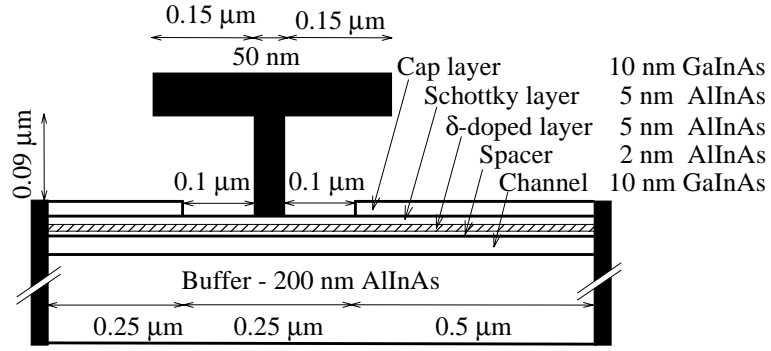


Fig. 1: Geometry of the simulated HEMT

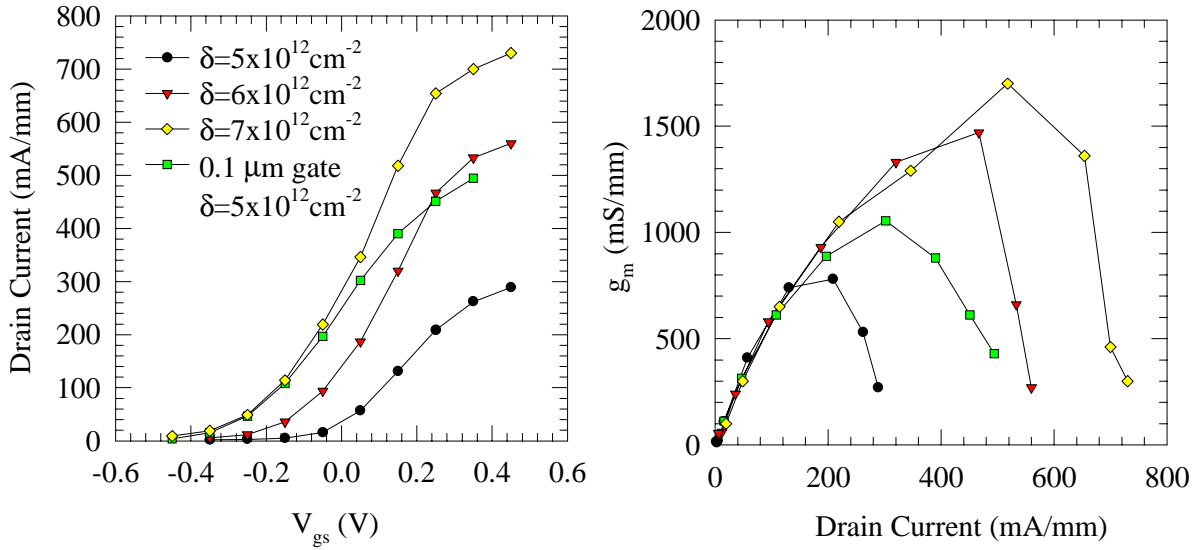


Fig. 2: Drain current vs. gate voltage and intrinsic transconductance vs. drain current for the 0.1 μm gate HEMT (squares) and the 50 nm gate HEMT with three different values of the δ -doping: $5 \times 10^{12} \text{ cm}^{-2}$ (circles), $6 \times 10^{12} \text{ cm}^{-2}$ (triangles) and $7 \times 10^{12} \text{ cm}^{-2}$ (diamonds). The drain voltage is 0.5 V and the gate built-in potential is taken to be 0.75 V.

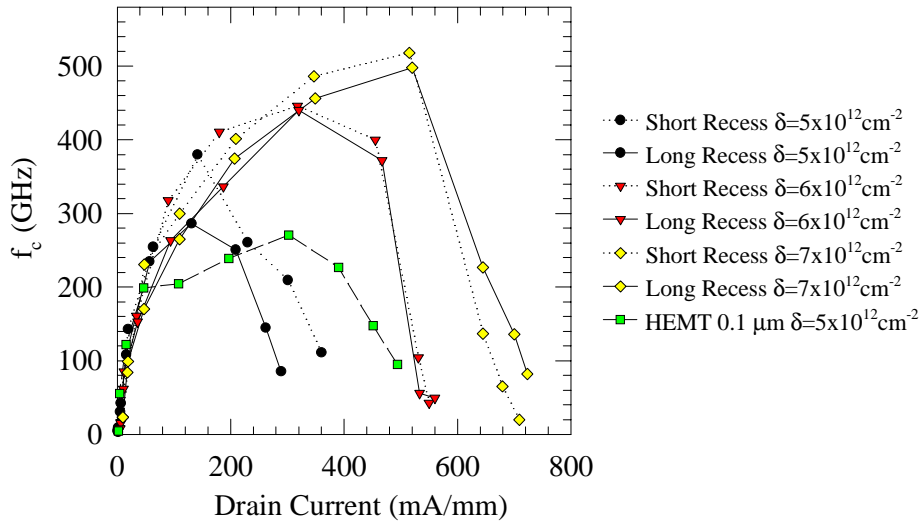


Fig. 3: Intrinsic cutoff frequency, f_c , as a function of drain current for the 0.1 μm gate HEMT and the 50 nm gate HEMT with three different values of the δ -doping: $5 \times 10^{12} \text{ cm}^{-2}$ (circles), $6 \times 10^{12} \text{ cm}^{-2}$ (triangles) and $7 \times 10^{12} \text{ cm}^{-2}$ (diamonds). Two different recess lengths have been used in the simulations of the 50 nm gate HEMT, a long one of 100 nm, as in Fig. 1 (solid lines) and a short one of 20 nm (dotted lines). The biasing is the same as in Fig. 2.