A NOVEL TOPOLOGY FOR A HEMT NEGATIVE CURRENT MIRROR

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ABSTRACT

A new solution for the implementation of a HEMT negative current source is presented. The topology can be also profitably employed as a current mirror and as an active load in high-gain MMICs voltage amplifiers. A small-signal model of the proposed circuit is developed which allows to find accurate expressions for the required transfer functions (i.e., the output impedance of the current source, and the current gain of the circuit when operated as a current mirror). Design examples using Philips PML ED02AH GaAs PHEMT process are provided. Spice simulations show that a 10-kW output impedance for the current source and a 35dB voltage gain for a differential pair loaded with the proposed current mirror are easily achieved.

INTRODUCTION

The lack of complementary devices in HEMT technology does not allow the usage of circuit topologies usually adopted in low frequency circuits. In particular, negative current sources, i.e. current sources driving loads connected to the negative bias rail, cannot be directly implemented. Thus, resistive loads are used in place of active ones, which could allow high voltage amplification without requiring high voltage supplies, as requested in low power ICs.
Several circuit topologies implementing negative current sources without employing complementary devices have been proposed for low frequency applications [Gilbert (1), Barker and Hart (2)]. More recently, an all-NPN negative current source suitable for RF monolithic transceivers has been presented in [Lantz and Floberg (3)].
In this communication a novel topology for a negative current source implemented in HEMT technology is proposed. The same circuit can be used as a current mirror with a high current amplification. Furthermore, it has been employed as an active load for a buffered differential amplifier obtaining a voltage gain as well as a bandwidth enhancement, compared to a differential pair with resistive load, under the same bias conditions.
An accurate small-signal model of the proposed topology has been also developed. Case studies for both the current source and the active loaded differential amplifier are carried out using ED02AH GaAs PHEMT process from Philips PML ($f_T \cong 63$GHz). Spice simulations show a 10kΩ output impedance up to 5GHz for the current source, and a 35dB voltage gain over a 5.5GHz bandwidth for the designed differential amplifier.

THE PROPOSED SOLUTION

The proposed negative current source (NCS) topology in shown in Figure 1. It is made up of a differential amplifier Q_1-Q_2 and R_{av}, two common drain transistors Q_3-Q_4, with buffering functions, and two resistors R_{sl}, R_{sr}. When the circuit is used as a current source [Figure 2.(a)], a variation ΔV_{out} of the nominal output voltage is amplified by the differential pair and the gate voltage of Q_1 is forced to follow V_{out}, thus resulting in a constant voltage drop across R_{sr}, which means a constant I_{out}. Assuming an infinite voltage gain of the differential pair, the expression of I_{out} is:

$$I_{out} = I_L \frac{R_{sl}}{R_{sr}} + \frac{V_{GS4}}{R_{sr}} . \quad (1)$$

In the current mirror applications [Figure 2.(b)], the current in R_{sl} is not fixed by a bias source, and an output current signal flows into the load resistance R_L when an input signal I_{test} is applied. In both applications, a voltage signal at the gate of Q_2 causes a signal with the same phase at the gate of Q_1 due negative feedback loop (provided by Q_3, Q_4 and R_{sl}). At the same time, a positive feedback signal is returned through Q_3 and resistance R_{sr}. The behavior of the circuit is affected by the compounded action of the two feedback loops, as it will be clear in next section where a block model is developed.
Figures 2.(c) and 2.(d) show the use of the current source and current mirror as active loads for an inverter and a differential pair, respectively. This last application will be considered in a case study in Section IV.

SMALL SIGNAL MODEL

Figure 3 shows a block diagram which models the small signal behavior of the NCS. The diagram can be used to obtain accurate expressions for the required transfer functions, i.e., the output impedance $z_{out}(s)$, of the current source, and the mirror current gain $A_I(s)$. Let A'_v be the voltage gain of the differential pair Q_1, Q_2 loaded with the Q_3 buffer input capacitance, C_{Q3}:

$$A'_v = \frac{1}{2} g_{m1,2} \frac{R_{av}}{1+sC_{Q_3}R_{av}} = \frac{A_v}{1+sC_{Q_3}R_{av}}, \tag{2}$$

and A'_{vf} the closed loop voltage gain of the dashed block in Figure 3:

$$A'_{v_f} = \frac{A'_v}{1+f_1 A'_v}, \tag{3}$$

where:

$$f_1 = \frac{z_{inl}}{z_{inl}+R_{sl}}. \tag{4}$$

From Figure 3, for the output impedance of the current source $z_{out}(s)$ we obtain:

$$z_{out}(s) = \frac{v_{out}}{i_{test}} = \frac{z_{inr} \| R_{sr}}{1-f_2 z_{inr} \| R_{sr} A'_{v_f}}, \tag{5}$$

where:

$$z_{inl} = \frac{1}{sC_{gs1}}, \tag{6}$$

$$z_{inr} = \frac{1}{sC_{gs2}}, \tag{7}$$

$$f_2 = \frac{1}{R_{sr}}. \tag{8}$$

In the same manner, the mirror current gain $A_I(s)$ is given by:

$$A_I(s) = \frac{i_{out}}{i_{test}} = \frac{f_1}{R_L} \frac{z_{inr} \| R_{sr} A'_{v_f}}{1-f_2 z_{inr} \| R_{sr} A'_{v_f}}, \tag{9}$$

where:

$$z_{inl} = \frac{1}{sC_{gs1}} \| R_L, \tag{10}$$

whereas z_{inr} and f_2 have the same expressions ((7), (8)) founded for the output impedance.
By substituting (3) in (5), (9) it follows:

$$z_{out}(s) = \frac{R_{sr}[(1+sC_{gs1}R_{sl})(1+sC_{Q_3}R_{av})+A_v]}{(1+sC_{gs2}R_{sr})[(1+sC_{gs1}R_{sl})(1+sC_{Q_3}R_{av})+A_v]-A_v(1+sC_{gs1}R_{sl})}, \quad (11)$$

$$A_I(s) = \frac{A_v R_{sr}/(R_{sl}+R_L)}{(1+sC_{gs2}R_{sr})[(1+sC_{gs1}R_{sl}\alpha_1)(1+sC_{Q_3}R_{av})+A_v\alpha_1]-A_v(1+sC_{gs1}R_{sl}\alpha_1)}, \quad (12)$$

where:

$$\alpha_1 = \frac{R_L}{R_{sl}+R_L}. \quad (13)$$

These last expressions constitute the required transfer functions and they can be studied by means of root locus technique in order to describe their frequency behavior under parameter variations.

CASE STUDIES

A SPICE simulation of the current source in Figure 2.(a), designed for I_{out} = 1mA (with V_{DD}=5V, R_{av}=3kΩ, R_{sl}=330Ω, R_{sr}=800Ω, I_{bias}=1mA, and I_L=1mA), is shown in Figure 4. The output resistance is about 10kΩ up to a frequency of 5GHz. The static transfer characteristic I_{out}-V_{out} is depicted in Figure 5, which shows the good current source behavior over a wide output voltage swing.
The voltage transfer gain of the active loaded differential pair (Figure 2.(d)) is shown in Figure 6: a 35dB gain over a 5.5GHz bandwidth is obtained. A comparison with a resistive loaded differential amplifier, using the same bias current (1mA) and power supply (5V), is also reported, showing the better performance of the proposed solution in terms of both gain and bandwidth.

CONCLUSIONS

In this paper a new topology for a HEMT negative current source has been presented which shows high output impedance over a wide bandwidth and a high signal-handling capability. The same topology can be used as a current mirror and it is employed as active load in a differential amplifier, obtaining a 35dB voltage gain over a 5.5GHz bandwidth. A small signal model of the proposed circuit has been developed which allows to carry out accurate expressions for the output impedance of the current source and the current mirror gain.

REFERENCES

[1] B. Gilbert, “Wideband Negative-Current Mirror”, Electronics Lett., vol. 11, no. 6.
[2] W. J. Barker, B. L. Hart, “Negative Current-Mirror Using n-p-n Transistors”, Electronics Lett., vol. 13, no. 11.
[3] M. Lantz, H. Floberg, “Bipolar, Wideband, Bias Current Source”, Proc. IEEE ISCAS ’99, 1999, pp. II208-II211.

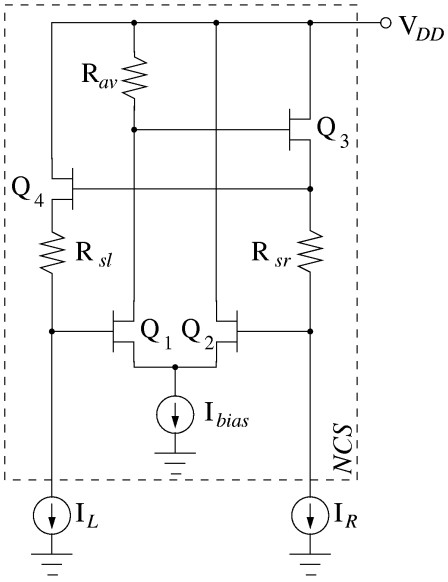

Figure 1 ¾ NCS topology.

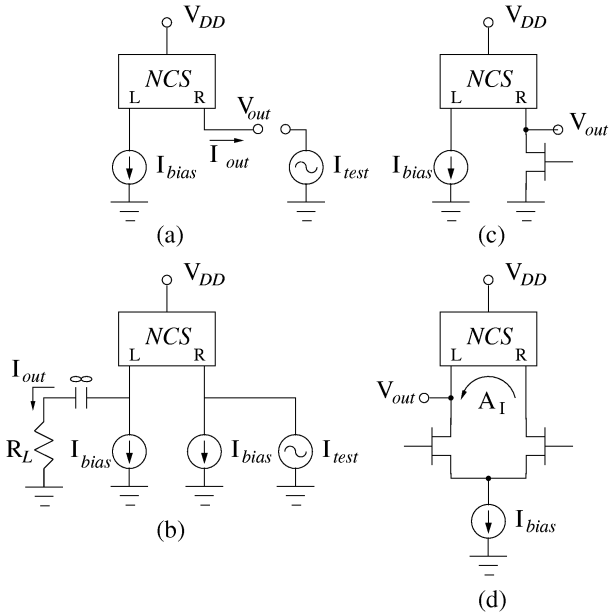

Figure 2 ¾ NCS applications.

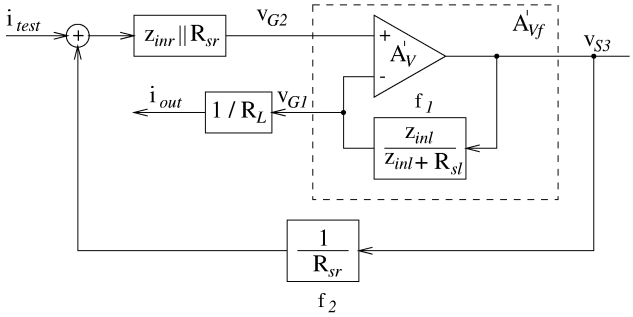

***Figure 3** ¾ Block diagram.*

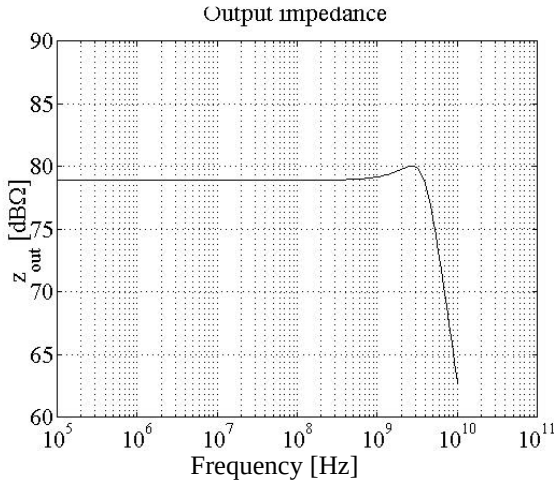

Figure 4 ¾ Current source output impedance.

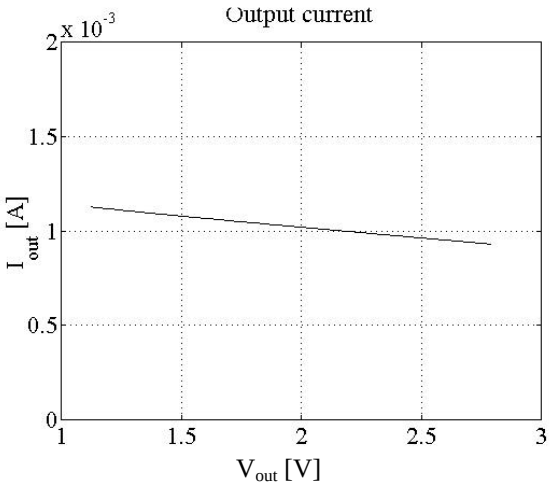

Figure 5 ¾ Static transfer characteristic.

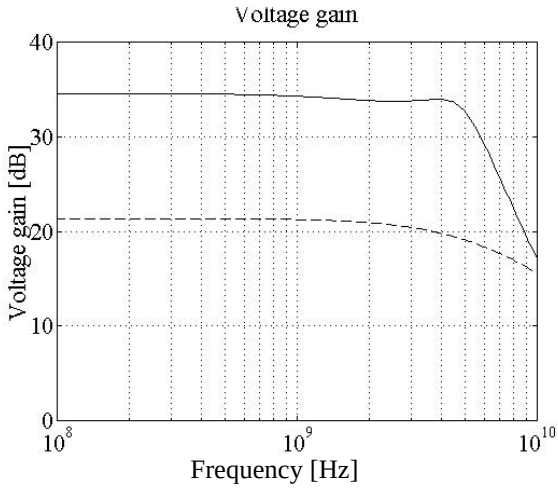

Figure 6 ¾ Resistive loaded (dashed) and NCS loaded (solid) differential pair voltage gain.