ACCURATE MICROWAVE CHARACTERISATION OF POWER LD-MOSFETs

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ABSTRACT

An accurate, non-quasi-static, non-linear equivalent circuit model of a power Si LD-MOSFET valid well into the microwave region has been extracted by means of a reliable and easy procedure. The model is intended for applications to high-efficiency power amplifiers in the low microwave region. The extraction is based on linear S-parameter measurements at many bias points with a hot-cold method for parasitic and intrinsic element determination. The model differs from the standard BSIM3 or MODEL9 models, ensuring accurate high-frequency performances.

I. INTRODUCTION

Si power LD-MOSFETs are currently investigated as possible candidates for power amplification in the lower microwave region, with applications e.g. in mobile communications of the third generation. The stringent requirements in terms of efficiency and linearity mandate the use of accurate models for the active device, valid well into the microwave region. The use of traditional models like the Berkeley BSIM3 or the Philips MODEL9 becomes questionable when non-quasi-static phenomena and fringing-field parasitics are significant, and affect the performance of the devices. Therefore a model derived from the high-frequency experience proves to be a better candidate for accurate high-frequency design, that requires at least some control of the harmonics of the signal, and a good prediction of distortion and intermodulation phenomena due also to non-linear reactances [1]. In the following a non-linear equivalent circuit and an accurate and reliable extraction procedure based on standard measurements are described for an LD-MOSFET from ST Microelectronics; the result show a good agreement between model and measurements. The model is currently used for the design of a high-efficiency power amplifier in L band.

II. THE EXTRACTION PROCEDURE

The device is a laterally-diffused (LD) MOSFET from ST Microelectronics, with a gate length of 0.3 μm, and a total gate periphery up to 7 mm. The measured device has 1.7 mm gate periphery with an I_{dss} of approx. 450 mA. The topology of the model is shown in fig.1, with the intrinsic (bias-dependent) elements enclosed by the dashed line. The extraction procedure is a modification of that described in [2], so that the specific features of the MOSFET are properly accounted for. The parasitic (bias-independent) elements are first evaluated at 'cold' conditions, i.e. with $V_{ds} = 0$, and then the intrinsic elements are evaluated at all bias conditions of interest, with the value of the parasitic obviously kept constant. The dependence of the intrinsic elements on the gate and drain voltages is then modelled by means of a suitable fitting function, fulfilling specific constraints of physical consistency [2]. The parasitics are evaluated at Vds = 0, with the gate voltage ranging from accumulation (V_{gs} = -4 V) to strong inversion (V_{gs} = 4 V); the threshold voltage is approximately V_T = 0.8 V. The parasitic inductances are first evaluated from the low-frequency slope *vs* frequency of the imaginary parts of the Z-parameters:

$$Im[Z_{11}] = j\omega(L_s + L_g) \qquad Im[Z_{12}] = Im[Z_{21}] = j\omega L_s \qquad Im[Z_{22}] = j\omega(L_s + L_d)$$

The dependence of the low-frequency slope of Im[Z_{11}] *vs* gate voltage is shown in fig. 2 as an example. The inductances are evaluated in the limit $V_{gs} \rightarrow +\infty$, where the influence of the capacitances and the RC-term correction are lowest [3]. The parasitic resistances are evaluated from the real parts of the Z-parameters:

$$Re[Z_{11}] = R_s + R_g \qquad Re[Z_{12}] = Re[Z_{21}] = R_s \qquad Re[Z_{22}] = R_s + R_d$$

The dependence of Re[Z_{22}] *vs* gate voltage is shown in fig. 3 as an example. The resistances are evaluated in the limit $V_{gs} \rightarrow +\infty$, where the channel resistance vanishes [2]. The parasitic capacitances are evaluated from the low-frequency slope *vs* frequency of the imaginary parts of the Y-parameters:

$$Im[Y_{11}] = j\omega(C_{pgd} + C_{pg}) \qquad Im[Y_{12}] = Im[Y_{21}] = -j\omega C_{pgd} \qquad Im[Y_{22}] = j\omega(C_{pgd} + C_{pd})$$

The dependence of the low-frequency slope of Im[Z_{22}] *vs* gate voltage is shown in fig. 3 as an example. The capacitances are evaluated at the minimum, where the channel is almost totally depleted, and before the accumulation begins. The intrinsic elements are now evaluated from measurements at all operating bias points of interest (V_{ds} = 0 ÷ 8 V , V_{gs} = 0 ÷ 3 V). A standard extraction procedure has been used as described in [2, 4, 5], that allows the explicit extraction of the values of the intrinsic elements at each bias point without the use of optimisers, after de-embedding of the parasitics. A comparison with the full S-parameters, as shown below, confirms the validity of the results. The extraction procedure is thus complete.

III. RESULTS AND CONCLUSIONS

The measured and modelled S-parameters of a power LD-MOSFET from ST Microelectronics with 1.7 mm total gate periphery are shown for several bias points. In fig.5 the S-parameters at a 'cold-FET' bias point (V_{ds} = 0 V, V_{gs} = 0 V) up to 10 GHz are shown. This bias point has been used essentially for low-frequency extraction of the parasitics. In fig. 6 the measured and modelled S-parameters at an operating bias point (V_{ds} = 2 V , V_{gs} = 1 V) are shown up to 20 GHz: the accuracy is very good up to a very high frequency. In fig. 7 the measured and modelled S-parameters at another operating bias point (V_{ds} = 3 V , V_{gs} = 1.5 V) are shown up to 20 GHz: once more the accuracy is very good up to a very high frequency.
In conclusion, an accurate, non-quasi-static equivalent circuit of a power LD-MOSFET for non-linear applications has been extracted, and an easy and reliable extraction procedure has been developed. The extraction is based on S-parameters measurements, and allows an easy identification of the intrinsic and parasitic elements of the equivalent circuit. Comparison with measured data shows the accuracy of the model well into the microwave region (20 GHz), ensuring reliable simulation results for non-linear design in the low and medium microwave frequency range.

IV. REFERENCES

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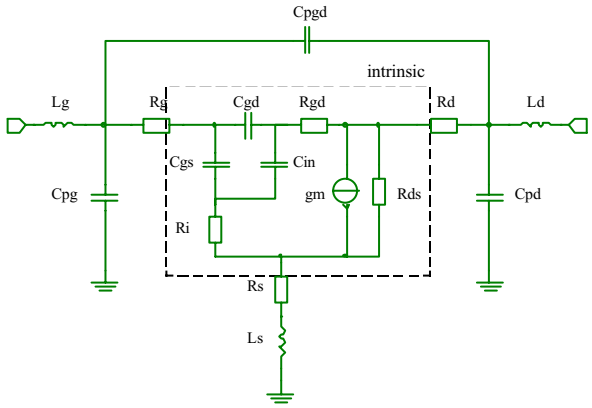

Fig.1 The Equivalent circuit of the MOSFET

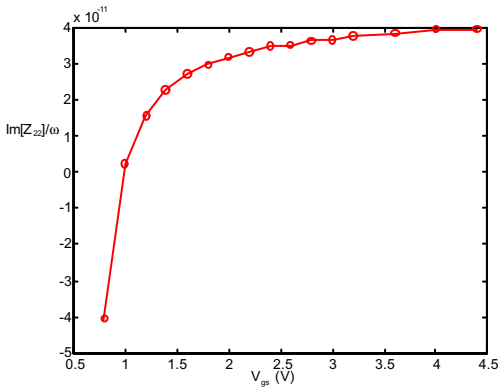

Fig.2 Low-frequency slope of the imaginary part of Z_{22} vs gate voltage

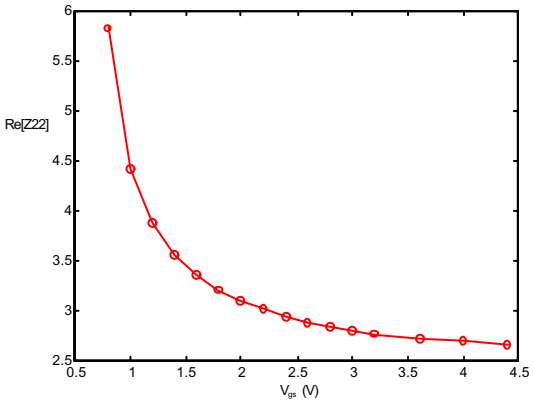

Fig.3 Real part of Z_{22} vs gate voltage

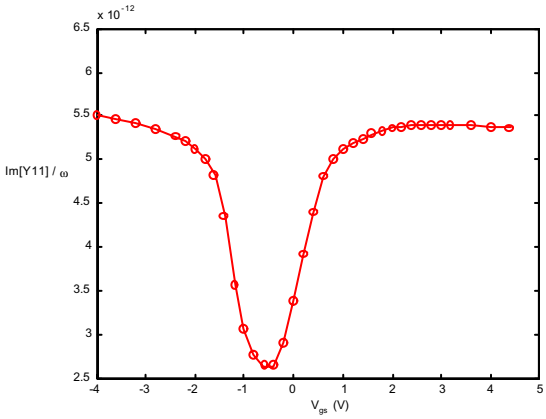

Fig.4 Low-frequency slope of the imaginary part of Y_{11} vs gate voltage

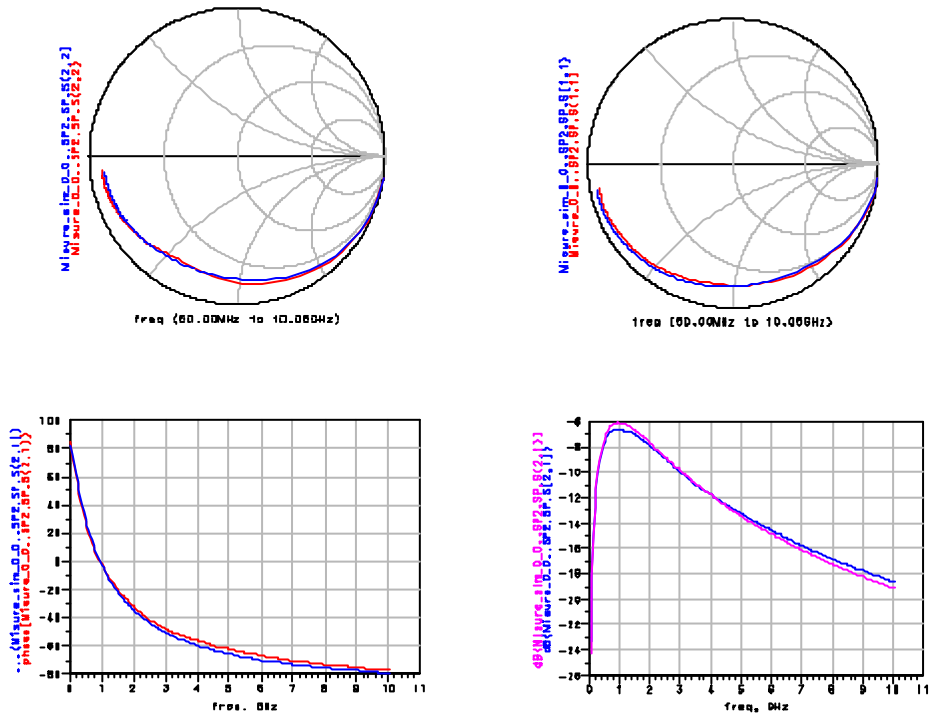

Fig.5 Measured and modelled S-parameters of the LD-MOSFET up to 10 GHz at V_{ds}=0 V, V_{gs}=0 V ('cold-FET'): S_{11}, S_{22}, S_{21} amplitude and phase.

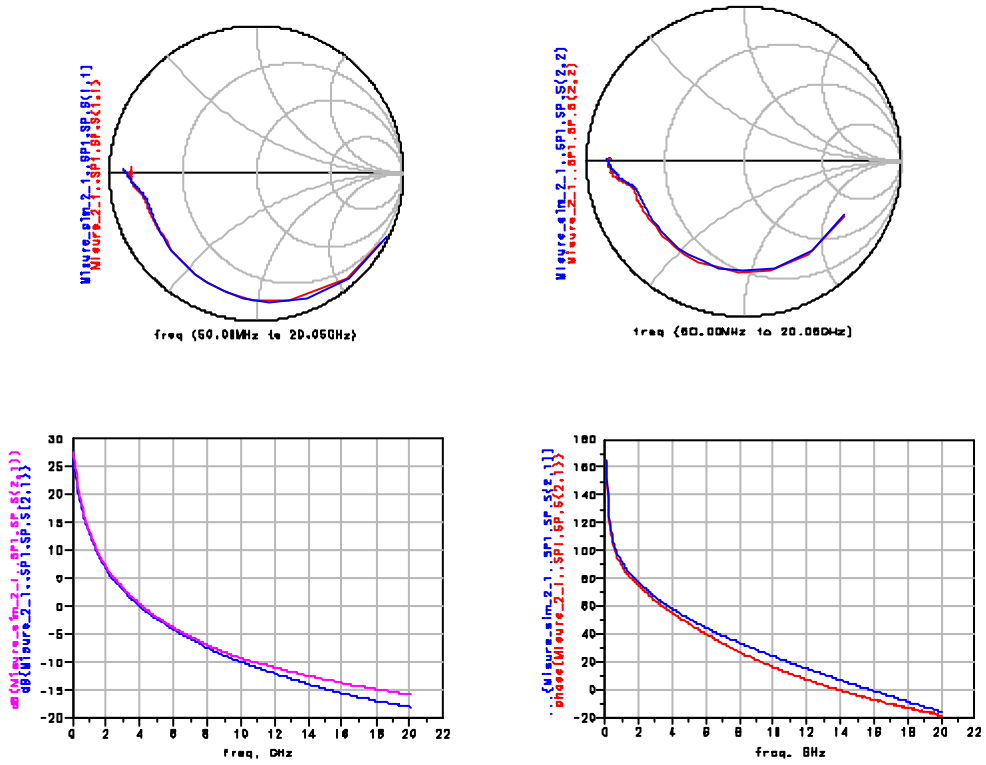

Fig.6 Measured and modelled S-parameters of the LD-MOSFET up to 20 GHz at V_{ds}=2 V, V_{gs}=1 V : S_{11}, S_{22}, S_{21} amplitude and phase.

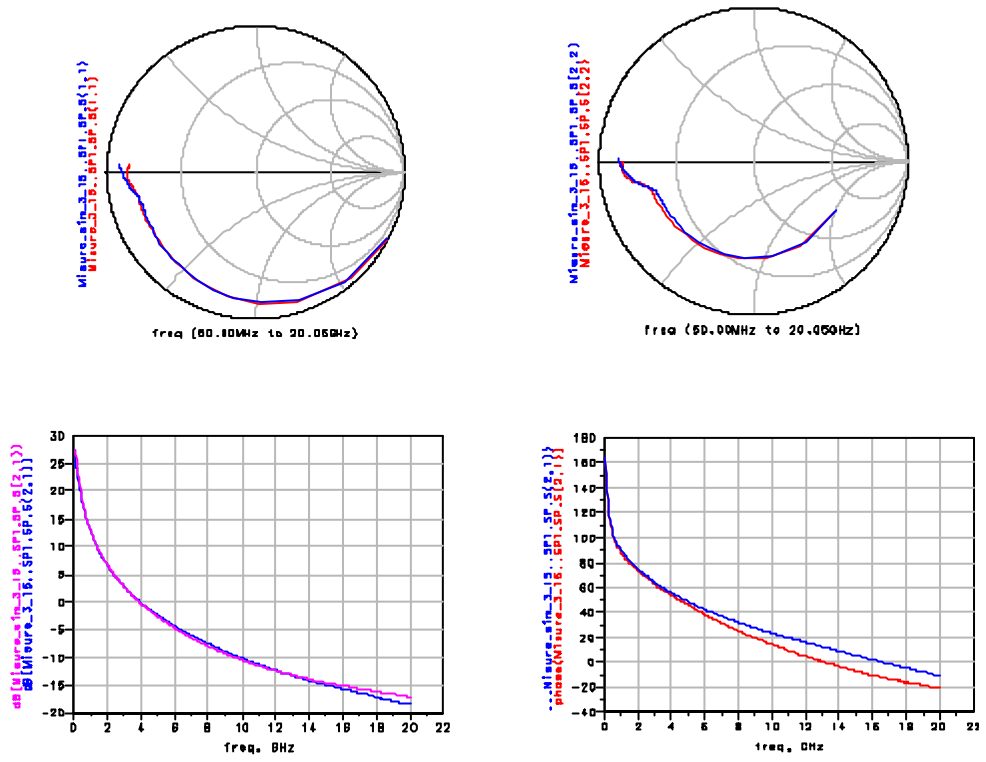

Fig.7 Measured and modelled S-parameters of the LD-MOSFET up to 20 GHz at V_{ds}=3 V, V_{gs}=1.5 V : S_{11}, S_{22}, S_{21} amplitude and phase.