

# Integrated Millimeter-Wave Silicon Micromachined Filters

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**Abstract** - This paper describes the design and the fabrication of a new type of millimeter-wave micromachined band pass filters, using silicon waveguides. The main interest of these components is their ability to be integrated along with other MMICs using flip chip bonding techniques. The micromachining fabrication technique allows to maintain very good fabrication tolerances, while the resulting filters are very compact. The design methodology is presented along with two examples of two and four pole filters at 42 GHz.

## I. INTRODUCTION

Flip chip assembly techniques appear to be a very promising solution for the construction of millimeter wave modules and sub-assemblies. It allows to obtain low loss and low parasitic interconnects and offers interesting properties for MMICs' thermal management. In these modules for example, filters are often required as front end preselectors. For these filters, the main requirements are low loss, compactness and easy integration. Planar filters are the best choice regarding integration and compactness, but they suffer from high losses and poor out of band rejection in the millimeter wave region.

On the other hand, waveguide filters offer superior performances but are difficult to connect with planar components, requiring precise mechanical machining to build transitions. Therefore, quasi planar components that can be directly interconnected with a planar passive network did receive much interest in the past few years[1]. In the same time, silicon bulk micromachining technique emerged as a promising solution to achieve collective precise machining that is required to build high Q monolithic resonant structures [2].

In this paper, we will present progress towards the development of a novel type of micromachined silicon waveguide filters in the 40 GHz frequency range, that can be easily integrated on any kind of substrate through flip chip bonding techniques.

We will first present the structure and the associated fabrication techniques, next the design methodology

applied to these filters and at last simulation results on 2 and 4 pole bandpass filters.

## II. STRUCTURE AND ASSOCIATED FABRICATION TECHNIQUES

At millimeter wave frequencies, high resistivity silicon loss tangent is known to be small enough to build planar structures having their loss dominated by top conductor line loss. Recently, experimental results on high resistivity silicon resonators [3] have shown that this material is also suitable to build high Q quasi planar resonators. Indeed, silicon loss tangent is decreasing with frequency, allowing to build high Q structures above 30 GHz. The filters presented below use this material as dielectric inserts in a micromachined waveguide. The structure is depicted in Fig. 1, and is very similar to conventional waveguide filters.

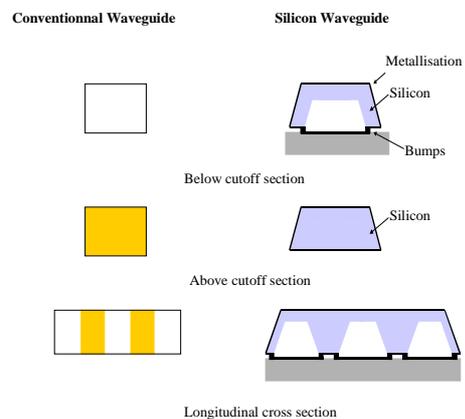


Figure 1. Comparison between a conventional waveguide filter and the proposed structure

The changes are that the sidewalls are no longer vertical, and that lower shielding in the evanescent sections is provided by a metal pad on the carrier substrate connected through a set of closely spaced bumps. The fundamental mode in this waveguide is a 'quasi'  $TE_{10}$  mode, since the sidewalls are changing the electric field orientation. The excitation is provided by a short circuited wide coplanar (CPW) line patterned on

the bottom side of the waveguide. This line is connected to a finite ground coplanar (FGC) line on the carrier substrate using bumps. The main interest of this structure is that both connection and fabrication are using collective processes and are therefore well suited for integration in millimeter wave sub-assemblies.

The fabrication process is based on successive front side and back side wet silicon etching (fig. 2) allowing to collectively build three-dimensional structures with machining tolerances in the micron range.

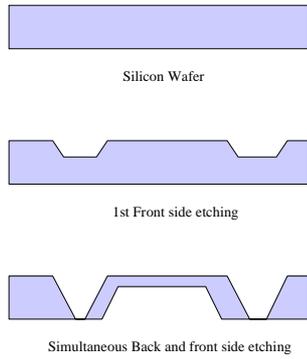


Figure 2. Fabrication principle of the waveguide

A detailed top view of the structure including mask layers is presented in fig. 3. The process starts on a high resistivity silicon wafer, covered with SiN layers on both sides. In a second step, the bottom side of the wafer is patterned to define the lower side copper metallization patterns, with evanescent sections and coupling slots defined. Next, a 10 micron thick BCB layer is deposited to grow the metallic pads on which the bumps are deposited. The SiN passivation layer is next opened on the front side of the wafer and a first selective 100  $\mu\text{m}$  deep etch is performed. The back side passivation is then removed and both sides are simultaneously etched until the waveguide structure is released.

Following this step, the front side is metallized, with side electroplated areas to ensure front to back side contact. At this point, the waveguides are ready to be bonded on the carrier substrate, where the input FGC lines and shielding plates have been patterned. The base of the waveguide is 1500  $\mu\text{m}$  wide and the wafer thickness is 525  $\mu\text{m}$ . The resonator length at the base is about 900  $\mu\text{m}$  in order to achieve resonant frequencies around 42 GHz, assuming that silicon has a permittivity equal to 11.6.

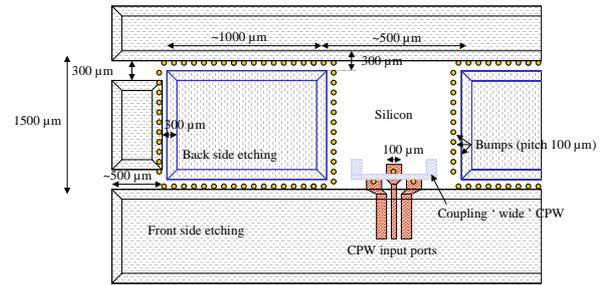


Figure 3. Detailed top view of the end and input sections.

### III. RESONATOR AND FILTER DESIGN

Since the structures cannot be tuned, the design relies heavily on 3D FEM rigorous modeling and associated filter design methodologies. The filter design methodology is based on the simulation of the resonator pairs to compute inter resonator couplings and of the input to compute the external Q. These two parameters can be determined from filter function prototypes and then computed using 3D full wave simulation tools. The design procedure will not be fully presented here, since it has been presented extensively in many papers in the past [4]. However, it is interesting to note that formulas for evanescent mode filters can not be applied in this case since the non vertical sidewalls and dielectric insert sides convert the quasi-TE<sub>10</sub> mode to TM modes. Still, we tried to maintain low computation time by using a segmentation approach for the simulations, while taking into account the non vertical sidewalls, and partially filled evanescent sections.

We divided the filters in three parts (see fig. 4): the end section, the input section and the resonators. Each section was simulated separately, but the resonator sections and the input sections used the same meshes, with different boundary conditions in the CPW coupling parts. This allows to minimize the frequency dispersion caused by different meshes related to each section.

Since the collective fabrication process requires to leave silicon suspension arms at the end of the components (see fig. 3), the filters cannot be completely shielded. Therefore, the end-section consists of an evanescent waveguide section, that allows to strongly attenuate the fields at the end of the structure

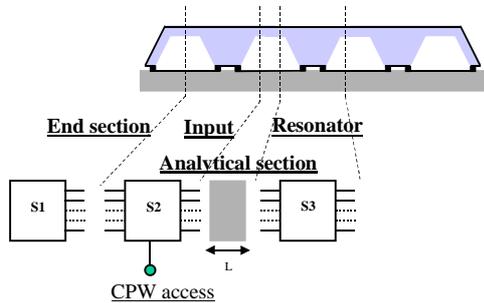


Figure 4. Methodology for FEM analysis of the structure.

The resonator section consists of a silicon-filled waveguide, between two evanescent sections. By using an appropriate generalized scattering matrix formulation, these parts can then be connected with the input access, taking into account several evanescent modes.

The input coupling structure has been carefully designed, since getting strong coupling to a cavity through a coupling slot is not straightforward. For our application, the targeted external  $Q$ s are in the range of 20, which has been obtained by using a wide, low impedance short circuited section of CPW line. This coupling method has proved to be very efficient, since such a wide line couples well to the substrate in the same way a wide CPW line triggers easily parasitic substrate modes. We could attain external  $Q$ s around 18 by using  $500 \mu\text{m}$  center-conductor wide CPW lines with  $100 \mu\text{m}$  wide gaps, on  $700 \mu\text{m}$  long by  $1500 \mu\text{m}$  wide resonator.

The three sections can be analyzed and tuned separately, while the evanescent section lengths can be analytically tuned and directly optimized to the desired values. From the filter standpoint, it means that this approach allows tuning the inter-resonator couplings without re-computing the whole structure.

#### IV. SIMULATION RESULTS

The targeted application of these filters is 5% band-pass filters around 42 GHz. We present here a set of two Chebyshev filters that were designed following the approach described in the previous section.

The two pole filter simulation results are presented on Fig. 5., where the targeted bandwidth has been obtained with a return loss better than 20 dB. The four pole filter simulation results are presented on Fig. 6. The return loss is better than 15 dB, with sharp out of

band rejection. Both filters have fractional bandwidth close to the targeted 5%, showing the validity of the design methodology.

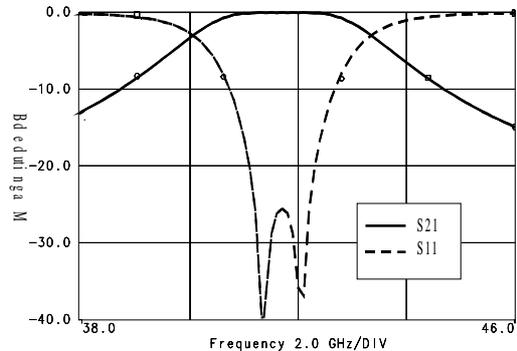


Figure 5. Simulated response of the two pole filter

The dimensions of the structures are about  $12 \times 3 \text{ mm}^2$  for the 4 pole filter, which compares very well with planar equivalents. Although losses are not taken into account in the presented simulation results, the computed unloaded  $Q$  of a single resonator is about 800 for the geometry presented on fig. 3. This will result in moderate insertion loss for medium bandwidth band pass filters.

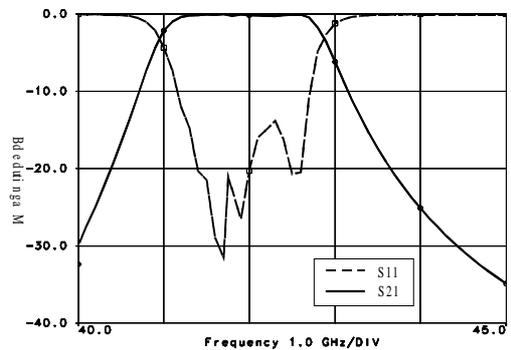


Figure 6. Simulated response of the four pole filter

These filters are currently under fabrication at LETI and experimental results on single resonators and several filters will be at the conference.

#### V. CONCLUSIONS

This paper describes the design and the fabrication of compact, integrated silicon micromachined filters. These filters are suitable for millimeter wave communication systems above 30 GHz, since the loss tangent of silicon is decreasing with frequency. They take advantage of the accuracy of micromachining techniques to attain the tolerances required at these

frequencies. Moreover, their integration in millimeter wave sub-assemblies is compatible with flip chip bonding techniques.

This work was supported by CNES under contract 1/98/7305.

## VI. REFERENCES

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