

# Single Chip 58 GHz Radio Relay Front End

Philippe Marchand, Philippe Gouessant

Alcatel CIT, Nanterre, France

**Abstract:** This article describes a solution for a low cost front end to be used in point to point radio relays operating in the uncoordinated 57.5 to 59 GHz frequency band. The main characteristics of the equipment operating in this band in Europe have recently been agreed in draft by the ETSI (December '99).

This standard favors the use of the Time Division Duplex (TDD) scheme that allows for the design of a very simple front end. Implementation of the equipment as a whole is also presented together with link measurement results.

## I. INTRODUCTION

### A. The 58 GHz uncoordinated band

In March 2000 the European Telecommunications Standards Institute issued the final draft of EN 300 408 (V1.2.1) in reference [1]. Basically this standard is one of the few dedicated to an uncoordinated band which means that users are free to implement and operate their own radio link without the lengthy band and channel allocation procedure.

The main characteristics are:

- Band: 57 GHz to 59 GHz
- Frequency etiquette to avoid interference from new links on links already in operation
- No specified duplex spacing
- EIRP < 15 dBW
- Maximum output power: 10 dBm
- Channel bandwidth:  $\pm 45$  MHz or  $\pm 25$  MHz
- No specified receiver performance

These basic requirements mean that design can be kept simple and inexpensive, as described below.

### B. The TDD mode

In Time Division Duplex mode the carrier frequency is shared between transmitter and receiver in a terminal equipment. The channel frequency is used alternately for transmission or reception, both link terminals being synchronized accordingly. This mode of operation brings two advantages:

- The duplexing of transmitter and receiver is greatly simplified; the transmitter can be switched off during reception and cannot degrade receiver performance during that period

- The frequency etiquette as requested by EN 300 408 is also simplified since only one frequency has to be selected on installation as opposed to the pair of frequencies required in a frequency division duplex (FDD) mode.

## II. PRINCIPLE OF THE ARCHITECTURE AND EQUIPMENT IMPLEMENTATION

One of the simplest architectures has been selected. For the transmitter a direct 2 or 4 FSK (according to the data rate) modulated oscillator is used. This synthesized oscillator operates at a rather low frequency around and below 2 GHz and is further multiplied by 32 up to the 60 GHz band. The receiver down-conversion reuses a portion of the transmit signal which, with the TDD mode, becomes a CW signal during the receive slots.

Usually a TDD front end requires a Transmit/Receive switch to connect the antenna port to the transmitter output or to the receiver input. To avoid the insertion loss of such a switch and simplify circuit design, a double polarized antenna is used, with the transmitter output connected to one polarization and the receiver input connected to the orthogonal polarization. To simplify installation of the equipment these polarizations are respectively oriented at  $+45^\circ$  and  $-45^\circ$  to the vertical. This means that there is no need to rotate one terminal by  $90^\circ$  relative to the other and the installation is the same for any terminal.

RF filtering in the front end is not needed, first because of the direct modulation scheme for the transmitter and second because the ETSI standard does not require any specific receiver selectivity.

Double-pol antenna

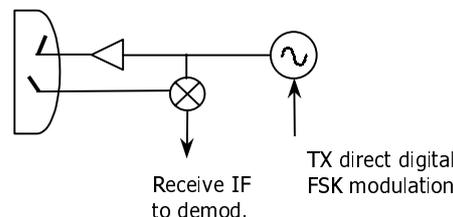


Fig. 1: Simplified block diagram

Such a solution, which is probably the simplest in terms of RF circuit complexity, is compatible with

single chip front-end integration. In the above simplified block diagram the receive IF frequency would be near zero for a pure TDD mode but could be a non-zero IF equal to the duplex spacing with a combination of TDD and FDD modes. To obtain a true TDD mode of operation, a shift mixer is inserted at the output of the local oscillator and a frequency shift is applied during the receive slots only. In the equipment the receive IF is 480 MHz to allow for low cost SAW filtering. Thus the frequency shift is  $480/32=15$  MHz (receive slots) or 0 (transmit slots – no spurious generation). This is achieved by means of a simple I/Q modulator placed at the output of the 2 GHz LO.

The antenna is a small offset parabola of 18 cm in diameter. The offset illumination has been selected because it allows the complete front end to be located and the focus without any blocking of radiated power. The measured gain is 37 dBi at 59 GHz. The ortho-mode transducer (OMT) is very simple and made with two orthogonal lines on an RT/duroid® substrate (Rogers Corporation, USA) that also acts as a sealing window for the small circular waveguide section ( $\text{Ø}3.5$  mm) to the conical horn feed. Indeed, here too, the TDD mode enables the ortho-mode transducer to be kept simple with moderate isolation performance in the order of 15 dB. Moreover the TX output amplifier is switched off during the receive slots to ensure that no residual noise degrades the receiver noise floor. This is achieved through the biasing circuit of the output amplifier stage. Insertion loss of the output coupling is below 1 dB and additional losses on the alumina substrate and wiring are also around 1 dB.

There is no microwave filtering and the equipment can be used over the whole frequency plan and at either end of any link.

The parabolic surface of the offset antenna is formed directly by one side of the equipment's die-cast housing and is therefore not detachable but manufactured at no additional cost. Behind this part of the housing, behind the parabolic section, a single printed circuit board carries all the data/base-band/IF processing and the power supply functions. Data processing includes a Reed-Solomon (RS: 128-112) forward error correcting code. This is embedded, together with the modem, into a single 350 kgate Si ASIC. The interface is a single coaxial cable of up to 200 meter long. The other end of this cable is connected to a small weatherproof unit that houses the two 2 Mbps (megabits per second) ITU-T G703 plesiochronous interfaces and an 84 – 265 VAC power supply for the terminal. The equipment can also be configured for single 2 Mbps traffic (1E1; 2.048 Mbps) or one or two 1.544 Mbps (1 or 2T1) streams for the North American applications above 59 GHz.

A separate unit can be added for a small battery pack to ensure uninterrupted link availability in case of mains failure for up to 15 minutes. The power consumption of the terminal is 20 W.



Fig 2: Front view of the complete transceiver, radome removed, front-end cover removed. The overall dimensions are approximately: 22 x 30 x 15 cm



Fig. 3: Upper rear view of the transceiver. Back plate removed. Main processing printed circuit board and (top) synthesizer board..

### III. FRONT END AND MMIC

The following block diagram shows the implementation principle of the front-end and also includes the block diagram of the MMIC chip.

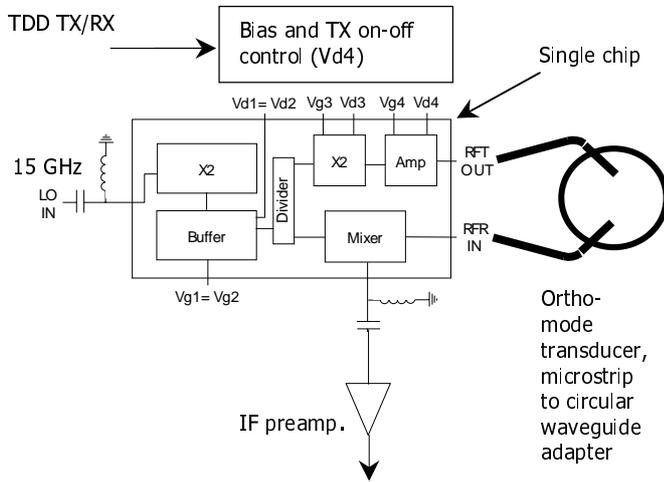


Fig.4; Block diagram of the front-end

The single chip includes the following functions:

- Local oscillator doubler from around 15 GHz to 30 GHz.
- LO buffer amplifier
- LO power divider to split the LO signal between TX and RX paths
- Sub-harmonically pumped down-converter with balanced IF outputs
- Second frequency doubler in the TX path, from around 30 GHz to 60 GHz
- TX output amplifier.

The main characteristics of the circuit are:

LO input power (14.3-14.75 GHz):	+12 dBm
IF RX frequency:	480 MHz
Noise figure (add 1 dB for IF preamp.):	11.5 dB
Power consumption:	1W
Chip size:	5.4 x 1.95mm <sup>2</sup> ; e=254μm

The technology is pHEMT 0.15 μm (four transistors and four diodes).

The circuit is flip-chip mounted on an alumina substrate (254 μm). To optimize the flip-chip assembly and to avoid the parasitic inductance of via holes, the design uses coplanar waveguide (CPW) at chip level. The flip-chip assembly makes use of stud-bumps with no underfill. The alumina substrate is preferred for the flip-chip assembly process and also includes a CPW to microstrip transition.

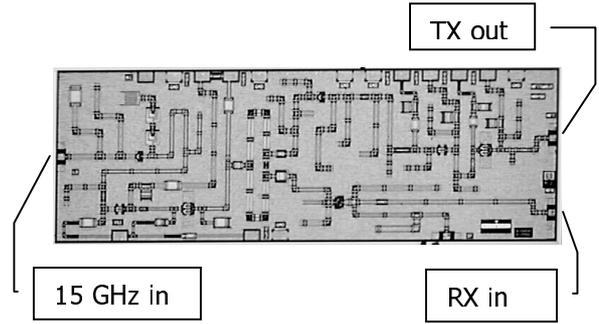


Fig.5: The TX/RX MMIC in CPW.

The two microstrip RF ports (TX and RX) of the alumina substrate are connected by short wires to a simple OMT made on thin organic substrate that also acts as a weatherproofing window for the circular waveguide output. The complete front end is housed in a weatherproof enclosure of 70 x 70 x 15 mm<sup>3</sup>.



Fig. 6: The front-end, cover plate removed. The OMT is clearly visible on the left (waveguide short circuit removed)

### IV. MEASUREMENT RESULTS.

#### A. At MMIC level

The MMIC characteristics have been measured in the band 57 to 59 GHz. An evaluation up to 60 GHz has also been performed and has given similar results.

Down-conversion losses:	< 11.5 dB
TX output power:	9.5 dBm < P < 11.5 dBm
RF port return loss:	< 9.5 dB

LO port RL: <12 dB  
Consumption: 990 mW

### B. At front-end level

Different front-ends have been measured within temperature range with the following main results:

TX output power at waveguide access: >7.5dBm  
RX noise figure at waveguide port: <14 dB  
(IF strip included)

### C. At data link level

At data link level the main measurement is the bit error ratio for different received levels. The link is measured with and without Reed-Solomon error correction to assess the intrinsic performances. The user data rate is 2x2 Mbps which corresponds to an aggregate data rate of 13.53 Mbps on the air interface due to the TDD mode and to the different additional data signals such as code redundancy, remote alarms, link identity code-word, etc.

BER	with RS code	w/o RS code
$10^{-3}$	-76.5 dBm	-75 dBm
$10^{-6}$	-75.8 dBm	-71 dBm

Received level vs. bit error ratio

FSK modulation with the RS coding is a very robust combination, and no sensitivity to shocks has been observed with the link remains error free under any ETSI standardized environmental conditions. Such performance levels are compatible with a good quality of service (link outage  $<5 \cdot 10^{-5}$  of the time on average per year) for applications with hop lengths between 1 to 2 km depending on the rain zone.

## V. CONCLUSION

A very inexpensive transceiver equipment has been developed based on the TDD mode that allows for simple millimeter-wave single chip solutions due to its method of non simultaneous transmission and reception. This has been applied at 58 GHz for a low cost compact radio relay for use in dense urban network; it is also very easy to install using an automatic frequency selection procedure.

The front-end is not only simple and cost-effective, but is small enough to be located at the focus of a parabolic dish.

## VI. ACKNOWLEDGEMENTS

The authors wish to thank all the team members of the various disciplines who participated in the design of the circuits and functions and in product integration.

The flip-chip assembly is made by our colleagues at Alcatel Space Industries, Toulouse, France.

And a special tribute to the pioneering work of Jagadis Chandra Bose at 60 GHz ( $\lambda = 5\text{mm}$ ); work done more than hundred years ago in 1897 [2].

## VII. REFERENCES

- [1] Draft ETSI EN 300 408 V1.2.1 (2000-03). "Fixed Radio Systems; Point-to-point equipment Parameters for digital radio systems for the transmission of digital signals and analogue video signals operating at around 58 GHz, which do not require co-ordinated frequency planning." ©European Telecommunications Standards Institute 2000.
- [2] A.K. Sen, "Sir J.C. Bose and Radio Science," IEEE MTT-S, 1997.