A WIDEBAND GAAS 6-BIT TRUE-TIME DELAY MMIC EMPLOYING ON-CHIP DIGITAL DRIVERS

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***Abstract* - This paper describes a 2-20 GHz 6-bit True-Time Delay. A total equivalent electrical length in air of 43.5 mm (145 ps) is achieved over a 2-20 GHz bandwidth. Digital drivers and a serial-to-parallel converter are integrated on the same MMIC. The ED02AH 0.2 μm PHEMT process from OMMIC is used. The time delay elements are realised using constant-R networks. The three smallest bits make use of a self-switched version of the constant-R networks while the 3 largest bits use a topology with single-pole double-throw (SPDT) switches and constant-R networks in the delay path. Measurement results for a typical chip are presented.**

I. INTRODUCTION

Active phased array antennas are nowadays being used for both radar and electronic warfare (EW) functions and therefore require a broadband behaviour. As such phased array antennas may contain many hundreds of transmit/receive modules, the application of MMIC's is mandatory for the reduction of antenna size, weight and cost. For narrowband applications, phase shifters are currently often being used. However, for broadband applications, they cannot be used due to "beam-squinting" effects which drastically influence the performance of a radar. The application of time-delay instead of a phase shift offers an enhanced broadband bandwidth with less "beam-squinting" effects. In this paper the design and the measured performance is described.

II. CONCEPT OF TRUE-TIME DELAY

In narrowband applications, phase shifters, which deliver a constant phase with frequency, are used to steer the antenna beam towards a certain angle θ with respect to the antenna aperture. Figure 1 displays a linear antenna array containing 4 radiating elements. The element spacing *d* is chosen equal to 15 mm.

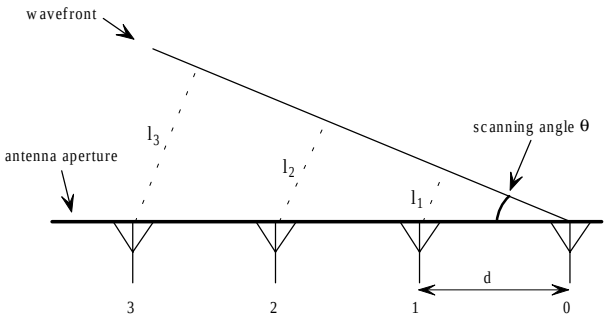

Figure 1: Linear array with 4 radiating elements.

The wavefront of the array is elevated under an angle θ with the antenna aperture. The distance l_1, l_2 or l_3 that each received signal has to travel before it arrives at the antenna aperture, depends on the scanning angle θ and the element spacing *d*. Following established theory [1], it can be shown that using a phase shift, which is proportional to the frequency, eliminates the "beam-squinting" effects which arise when using conventional phase shifters. A True-Time Delay element exhibits such a phase behaviour and is therefore preferred for a wideband phased array antenna.

The required number of bits for the True-Time Delay is calculated using the minimum and maximum required scan angle θ. To obtain a minimum scan angle θ_{min} of approximately 3 degrees the minimum additional distance l_1 in air which the signal needs to travel to arrive at the antenna aperture, is given by:

$$l_1 = d\ \sin(\theta_{min}) = 0.79\ mm \qquad (1)$$

A maximum scan angle θ_{max} of approximately 60 degrees is achieved by introducing the maximum distance in air to the antenna element on the far end of the linear array. The distance l_3 is given by:

$$l_3 = 3d\ \sin(\theta_{max}) = 39.0\ mm \qquad (2)$$

The number of binary bits which is required to deliver a

scan angle between 3 and 60 degrees can now be calculated:

$$l_3 = l_1 \, 2^n \qquad (3)$$

with *n* the number of bits. For the considered antenna array, a total number of 6 bits is required. Table I lists the equivalent electrical lengths which were used for the design of the 6-bit True-Time Delay. The equivalent time delay of each bit is also given.

Table I: specified equivalent electrical lengths and delays

Bit:	Electrical length (in air) [mm]:	Delay [ps]:
1	0.75	2.5
2	1.5	5.0
3	3.0	10.0
4	6.0	20.0
5	12.0	40.0
6	24.0	80.0

When considering larger antenna arrays, the number of bits normally can be reduced at the cost of larger phase errors which result in a slightly worse side-lobe level.

III. CONSTANT-R NETWORKS

To reduce chip dimensions, the concept of constant-R networks has been employed for the delay bits. Established theory [2] shows that the maximum achievable delay for a single constant-R network at a cut-off frequency of 20 GHz is approximately 16 ps. For larger delays, the cut-off frequency is below 20 GHz. Therefore, a single constant-R networks is only applied for bits 1, 2 and 3. Figure 2 gives the topology of a self-switched constant-R network that contains two FET's which are driven complementary to each other.

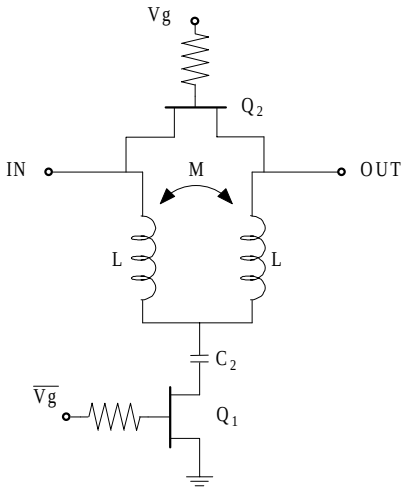

Figure 2: Topology of a self-switched constant-R network.

When compared with the conventional approach which uses SPDT switches, this topology has the advantage of a lower insertion loss and a smaller occupied area. As an initial guess, the design equations in [2] are used. The coupled inductances are realised using coupled microstrip lines. Due to the small dimensions involved, the passive part of the structure has been simulated inside a planar electromagnetic simulator (Momentum from Agilent Technologies) to account for the inevitable coupling. Careful choice of the FET dimensions and the spacing between the microstrip lines is required to obtain a flat time delay over frequency. Obtaining an extremely flat time delay will however have a negative influence on the insertion loss and return loss of the considered bit. The optimised layout of bit 1 is shown in figure 3.

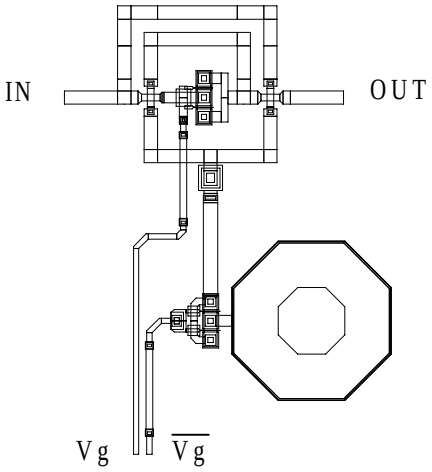

Figure 3: Layout of bit 1 (300 x 210 μm^2).

For bits 4, 5 and 6 the conventional single-pole double-throw (SPDT) configuration is used. The disadvantage of the SPDT configuration are the high losses which are caused by the 4 switches which are needed to switch between the delay and reference path and the additional 4 switches which are used to improve the isolation. The delay elements are constant-R networks which enable a flat time delay over a wide frequency band. Cascading separate constant-R networks increases the total time-delay and is therefore used for bit 5 and 6. The layout of the largest bit (bit 6) is depicted in figure 4.

Again, extensive planar electromagnetic simulations have been performed on the constant-R networks inside bit 4, 5 and 6. The complete 6-bit True-Time Delay is compiled by simply cascading the 6 separate bits. The on-chip bit sequence is dictated by the available space on the chip and is not optimised for the matching between the separate bits.

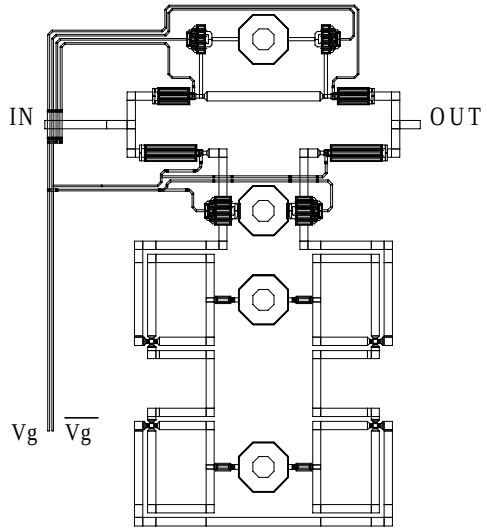

Figure 4: Layout of bit 6 (640 x 1250 µm^2).

IV. 6-BIT DIGITAL CONTROL

In order to improve the chip integration, a 6-bit digital driver has been incorporated with the True-Time Delay. The digital circuitry consists of 6 shift registers and some additional circuitry to generate the clock and perform the conversion from external TTL level to the internal Direct Coupled Fet Logic (DCFL) which is used on-chip. A functional block diagram is given in figure 5. Each shift register contains three D flip-flops and a driver which is used to drive the RF switches. Both complementary switching voltages (0 V and -1.5 V) are available at the output of the driver. The layout of the shift register is designed in such a way that it can be easily cascaded. Therefore, it can be adopted for designs with an arbitrary number of bits.

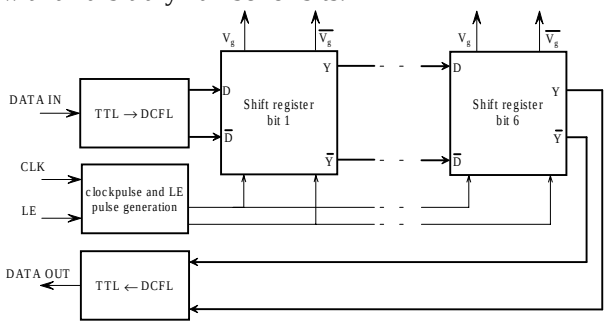

Figure 5: Functional block diagram of the digital on-chip circuitry.

Supply voltages of +5V, +2.5V and -5V are needed for the digital circuitry. The total DC power consumption is less than 30 mW for 6 shift registers and the necessary additional on-chip circuitry. During measurements, a serial bitstream was clocked into the digital circuitry (DATA IN) using a standard personal computer. The DATA OUT bitstream is available on-chip and can be fed to a second chip or it can be used for testing purposes. The digital drivers have been tested with a clockspeed of 100 kHz but are expected to work with a maximum clockspeed of 20 MHz.

V. MEASUREMENT RESULTS

A photograph of the realised True-Time Delay with 6-bit digital driver is given in figure 6. The occupied area is 4.0 x 1.4 mm^2.

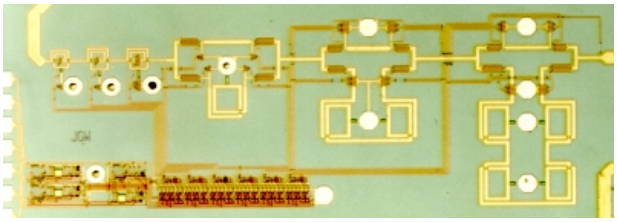

Figure 6: Photograph of the 6-bit True-Time Delay (4.0 x 1.4 mm^2).

The connection pads for the digital control are situated at the left side of the chip. Please note the small size of the 3 self-switched constant-R networks compared to the size of the 3 SPDT-based delay bits.

For a typical chip, the measured equivalent electrical length in air for all 63 states is given in figure 7 where the zero delay state is the reference state.

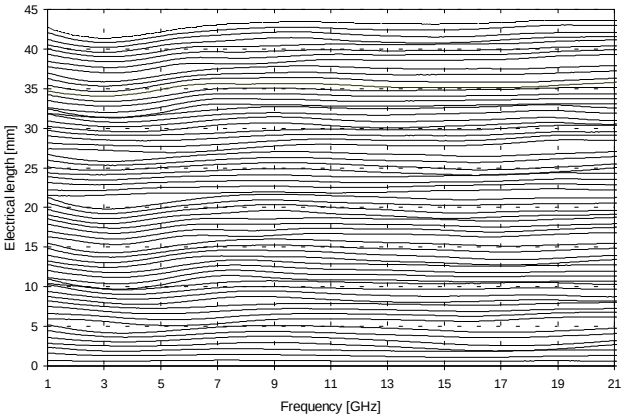

Figure 7: Measured equivalent electrical length relative to the zero delay state.

The realised electrical lengths are very flat as a function of frequency. The total achievable electrical length is equal to 43.5 mm which is 10% lower than the target specifications. A further investigation of teststructures, which were added to the wafer to evaluate the separate bits, revealed an offset in the electrical lengths of all the bits. This offset is probably caused by the neglection of the edge-coupling between the closely spaced microstrip

lines within the constant-R networks. The utilised planar electromagnetic simulator is unable to take this coupling into account.

When using the True-Time Delay MMIC, it is possible to correct for the actual delay values. In an actual application, this approach requires a *look-up table* which maps all required delays to the available bitstates. Doing so, we are able to calculate the RMS error for each of the 63 bitstates. The results for these calculations are given in figure 8. From figure 8 it is concluded that the maximum RMS error is equal to 0.68 mm which is almost equal to the LSB of the realised 6-bit True-Time Delay (LSB = 0.65 mm).

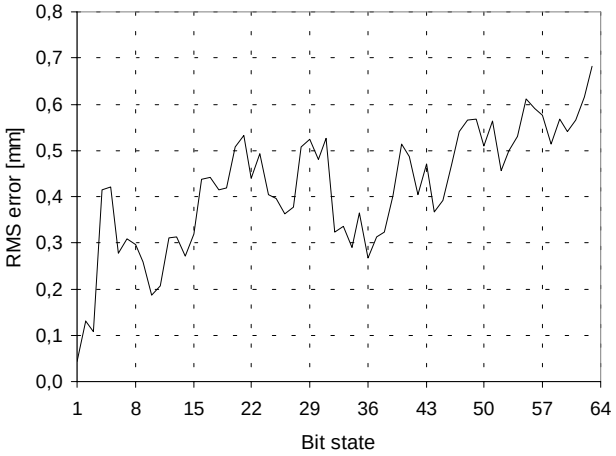

Figure 8: RMS error for all bitstates (2-20GHz).

The insertion loss of the True-Time Delay as a function of frequency for all 63 states is given in figure 9.

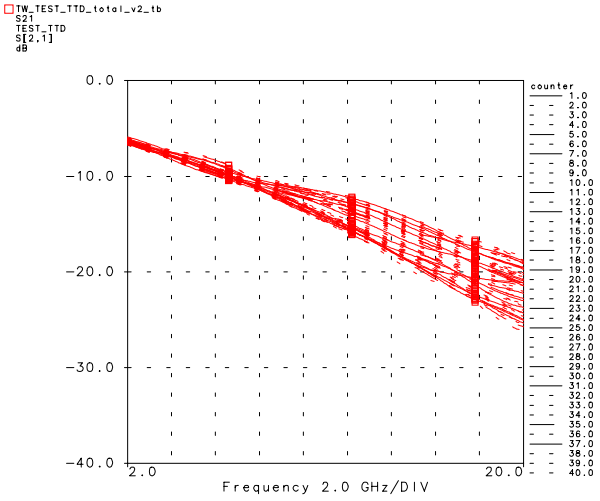

Figure 9: Measured insertion loss [dB] for all 63 states.

A linear array (see figure 1) is employed to give an impression of the "beam-squint" effects when using the realised True-Time Delay. The 4 radiating elements are considered to be isotropic while the distance *d* between them is equal to 15 mm. We compare the *'actual'* beam direction of the array with the *'nominal'* beam direction which occurs when the True-Time Delay is considered ideal. Figure 10 gives the results for a scanning angle θ of respectively 5° and 54°.

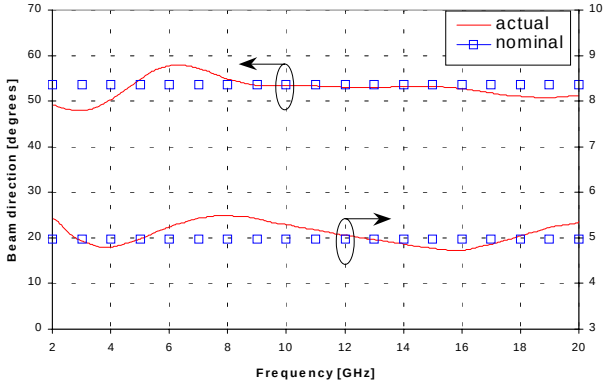

Figure 10: Beam squint at $\theta = 5°$ and $54°$.

Differences between the *'nominal'* and *'actual'* beam direction are caused by the small fluctuations which are observed in the equivalent electrical length of the states (see figure 7). Considering the relation between aperture size (in wavelength) and beamwidth, any differences in delay will have a relatively larger impact at higher frequencies than at lower frequencies. The observed differences in the beam direction can therefore considered to be small.

VI. CONCLUSIONS

A 2-20 GHz 6 bit True-Time Delay with a maximum equivalent electrical length of 43.5 mm (145 ps) has been presented for wideband active phased array applications. The use of self-switched constant-R network allows a small bit size and a lower insertion loss when compared to the conventional SPDT topology. The maximum achievable delay is however limited and therefore the 3 largest bits are realised using a conventional SPDT configuration with constant-R networks as delay elements. A 6 bit on-chip digital driver controls all the switches inside the True-Time Delay and is fed by an external TTL signal. The MMIC is considered state-of-the-art especially with respect to the flatness of the implemented True-Time Delay.

VII. REFERENCES

[1] R. J. Mailloux, *Phased Array Antenna Handbook*, Boston London, Artech House, 1993

[2] A. Ouacha and B. Carlegrim, "MMIC Self-Switched Time Shifter For Broadband Applications", *Microwave And Optical Technology Letters* , pp. 15 - 20, September 1998