Regenerative GaAs MMIC Frequency Dividers for 28 and 14 GHz

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***Abstract* — The design and characterization of two regenerative frequency dividers based on a commercial foundry GaAs HEMT-process are described. The dividers are intended to be used in a 56 GHz phase locked frequency generator. The main goal is to design dividers that have high input sensitivity and low DC-power consumption. The dividers are regenerative and consist of a resistive mixer followed by a frequency selective amplifier. The regenerative divider, compared to a digital divider, consumes less DC-power and has a higher operational frequency. The output of the amplifier is fed back into the LO-port of the mixer through a lumped element coupler. The dividers occupy 4.5 mm^2 each. Both dividers deliver 7 dBm output power with a rejection of the fundamental frequency of more than 15 dB and a DC-power consumption of 100 mW. The 14 GHz and 28 GHz dividers have 3 dB bandwidths of 11% and 5.7% respectively.**

I. Introduction

Frequency dividers are primarily used in phase locked frequency generators with higher frequency than available frequency references. The divider is used to transform the ouput signal of the generator to a frequency where a reference exists. The lack of phase/frequency discriminators in the millimeter wave band also explains the need for frequency dividers. Frequency division can be obtained by using a digital or an analog approach. The digital dividers can be either static or dynamic. The static divider is usually a D-latch with the complementary output fed back to the input. The static divider has a large bandwidth from almost DC level. The dynamic divider could be a ring oscillator with one inverter and one transmission gate. The dynamic divider, compared to the static divider, has a higher maximum frequency of operation but narrower bandwidth. Digital dividers using GaAs HEMT devices are described in [1]. The analog frequency divider uses a mixer with the IF fed back to the LO. The divider, called Miller-divider, was first described in [2]. A single transistor solution was proposed in [3] and also described in [4]. A solution with separate mixer and amplifier is described in [5,6]. This paper describes two frequencies dividers designed using a 0.15 µm GaAs PHEMT process. The dividers are supposed to be used in a 56 GHz phase locked frequency source and operate at 1/2 and 1/4 of the generator frequency.

II. Divider design

A schematic view of the divider circuit is shown in Fig. 1. The input is connected to the RF-port of a resistive mixer. In order to get reasonable signal levels, the IF is fed to a bandpass amplifier, optimized to amplify the frequency, $f_{in}/2$, and suppress the second possible locking frequency, $3f_{in}/2$. The output signal of the amplifier is fed to a coupler that couples -10 dB of the signal back to the LO-port of the mixer. To keep the size down, the whole circuit has been implemented with lumped elements. There are three DC-biases applied to the circuit, one for the gate bias of the mixer and two for gate and drain bias of the amplifier. The chip size is 1.5×3 mm^2 which can be easily reduced to a smaller size. A photo of the 14 GHz chip is shown Fig. 2 below. The 28 GHz chip has the same structure.

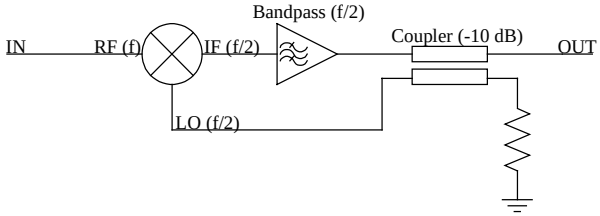

Figure 1. Schematic view of the divider circuit

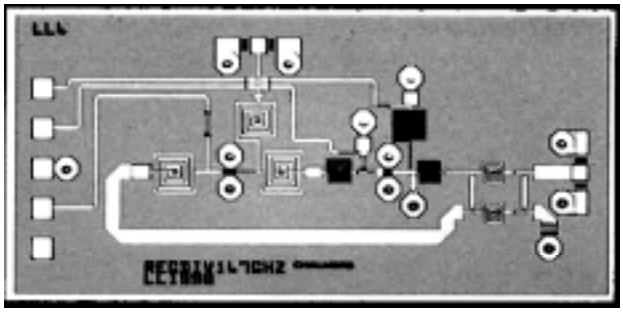

Figure 2. Chip layout for the 14 GHz divider

III. Simulation results

The frequency divider was simulated using MDS [7] and the foundry, Philips Microwave Limeil, provided the models of the components. The transistor technology is based on a depletion HEMT process, D01PH. This process has transistors with gatelength of 0.15 µm and an f_T of 95 GHz. The most critical part of the circuit is the mixer and the most important parameter is the leakage signal from the LO- to the IF-port. If the leakage is not small enough it would be hard to stop the circuit from oscillating when the input signal is absent. The performance of the mixer was optimized with respect to the LO-leakage and the conversion gain. The simulation of the 14 GHz mixer showed that a conversion gain around -7 dBm and a LO-leakage of -17 dB could be expected. The simulations of the IF amplifier following the mixer showed that a gain of 10 dB at the design

frequency, 7 GHz, and a sufficient suppression of the second possible locking frequency, 21 GHz could be expected. The coupler consists of two lumped capacitors and two lumped inductors. It is designed to couple -10 dB of the output signal back to the LO-port. The simulation of the 28 GHz mixer predicted a conversion loss of 9 dB. The 14 GHz amplifier was designed to provide 12 dB gain at 14 GHz and sufficient suppression of the 42 GHz tone. After the design of the different circuit elements some efforts were done to simulate the complete circuit. Since the frequency component at half the frequency is not present naturally in the circuit at startup, noise power at half the input frequency needs to be inserted into the LO-path. Then the power level of the noise signal is increased step by step until a large change in the divider output power is observed. This change can not only be explained by the induced noise signal. The conclusion is that the circuit starts dividing the input frequency. The conversion of the divider is difficult to determine from this simulation since the circuit was stimulated with a signal injected in the LO-path. By adding the gain of the mixer to the gain of the amplifier an estimate of the total conversion gain can be made. This means that both dividers should have conversion gain of approximately 3 dB at 0 dBm input power.

IV. Experimental Results

The experimental verification has been performed using on-chip power measurements utilizing coplanar probing techniques. The output power was measured by using a HP 83650A generator and a HP 8565E spectrum analyzer. The 14 GHz divider frequency response is shown in Fig. 3.The. The maximum conversion gain is 3 dB, the maximum output power is 7 dBm, the 3 dB bandwidth is 11 % and the rejection of the fundamental frequency at the output is better than 15 dB over the input power range. The total DC-power consumption is 100 mW. The 28 GHz divider has a total DC-power consumption of 100 mW. A power sweep is shown in Fig. 4. The maximum conversion gain is 3 dB, the maximum output power is 7 dBm, the 3 dB bandwidth is 5.7 % and the rejection of the fundamental frequency at the output is better than 15 dB over the input power range. The DC-power consumption is quite high and could be decreased by a re-design of the amplifier stage, still the DC-power consumption is lower than corresponding digtal solutions.

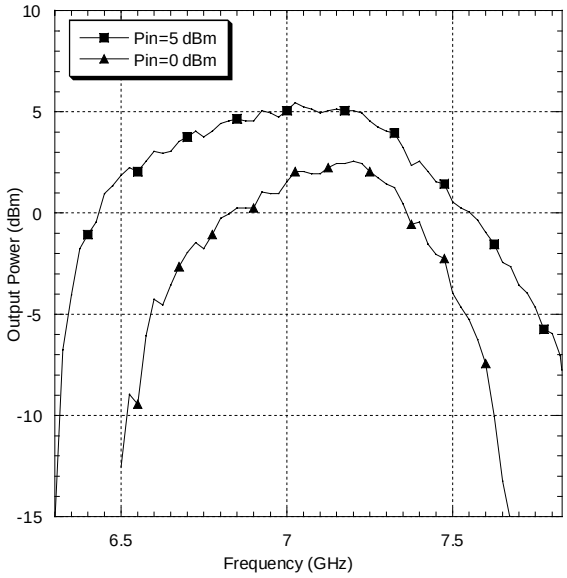

Figure 3. Frequency response for the 14 GHz divider. The bias condition is $V_{gs,mix}$=-0.5 V, $V_{gs,amp}$=0 V, and $V_{ds,amp}$=2 V

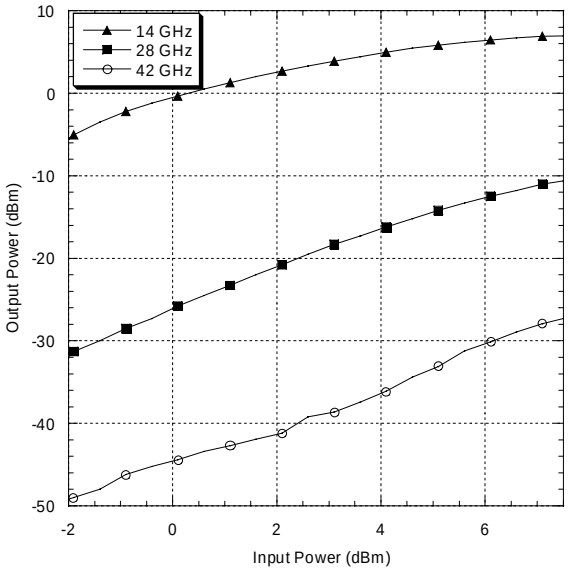

Figure 4. Power sweep for the 28 GHz divider. The bias condition is $V_{gs,mix}$=-0.5 V, $V_{gs,amp}$=-0.5 V, and $V_{ds,amp}$=2 V

V. Summary

Two MMIC regenerative frequency dividers, one for 14 GHz and one for 28 GHz, have been designed, simulated, and characterized. The dividers are intended to be used in a 56 GHz phase locked frequency generator. The design goals were low DC-power consumption and high input sensitivity. This is why the regenerative frequency divider approach was chosen. The DC-power consumption is quite high, 100 mW for both dividers, due

to an overdimensioned amplifier stage, but the DC-consumption is still lower than corresponding digital solutions. The maximum output power is 7 dBm for both dividers. The 3 dB bandwidth is 11% for the 14 GHz divider and 5.7% for the 28 GHz divider. Good agreement between the measured and the predicted simulated performance was obtained. Future upgrades include decrease of the power consumption, decrease of the chip size and an attempt of making dividers for higher frequencies.

VI. Acknowledgement

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VII. References

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