Two Octave Phemt Power Amplifier for EW Applications

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***Abstract* – Two 4.5-18 GHz MMIC amplifiers have been designed and fully tested. They have been fabricated using the Power pHemt process available at TriQuint Semiconductor, Texas. The first amplifier is a one stage distributed power amplifier which has been power optimised and exhibits 1W CW output power for a 6 dB associated gain. The second amplifier is a 2W three stage power amplifier with 20 dB gain. They are part of a first run launched in order to evaluate the different wideband structures and to improve linear and non linear models.**

I. INTRODUCTION

Electronic Warfare applications require very wide band MMIC amplifiers. Criteria like maximum power and maximum efficiency, but also high reliability and high integration, are some of the most important issues. In this context, MESFET technology has shown some good results [1], but is still limited in efficiency and gain at high frequencies. HBT technology has demonstrated the best results in power density and some good results in achieving wide band performance [2, 3]. Limitations for this technology are poor gain per stage and low impedance operation. PHemt technology has already demonstrated very good results in achieving wide band and high power levels associated with high gain [5, 6, 7]. Nowadays, it seems to be the best candidate for the 2 octave frequency band operation. The process used is the 0.25µm TriQuint Texas Power pHemt process which is commercially available. It has already supported many developments in the 6-18 GHz frequency band.

The designs presented below take place in a study supported by French Administration in order to evaluate the most suitable technology for airborne radars and electronic warfare applications. Thus a X band power amplifier has been also developped and exhibits quite good performance with 39 dBm output power, 17 dB associated gain and 40% PAE (power added efficiency).

II. POWER AMPLIFIERS

A. One Watt Class Distributed Power Amplifier

The best topology for wide band applications is the travelling-wave amplifier which overcomes limitations in the gain-bandwidth product by absorbing gate and drain capacitors into artificial transmission lines. But, conventional distributed amplifiers based on small signal design are not suitable for maximum power operation. The 1 W amplifier presented in this paper has been designed using a methodology based on a large signal approach [1, 2]. This methodology is based on a specific tapering of gate and drain lines omitting the drain load to optimise power operation. The circuit schematic is presented in Figure 1. Six cells have been used for the amplifier which has a 2.1 mm total gate width. The first transistor is affected by the drain load and does not provide maximum output power. A 600µm FET has been chosen to facilitate the power matching of the 5 following cells which are 300µm FETs optimised for power operation.

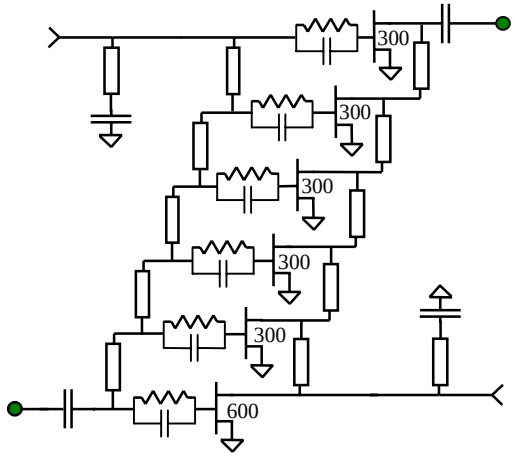
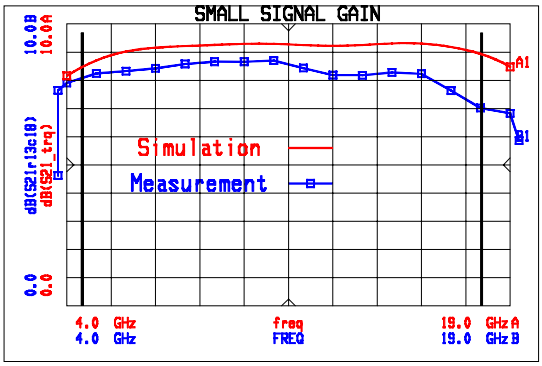


Figure 1 : One stage Distributed Amplifier schematic

Typical simulated [S] parameters are shown. These simulated performances were obtained using the small-signal models from TriQuint.



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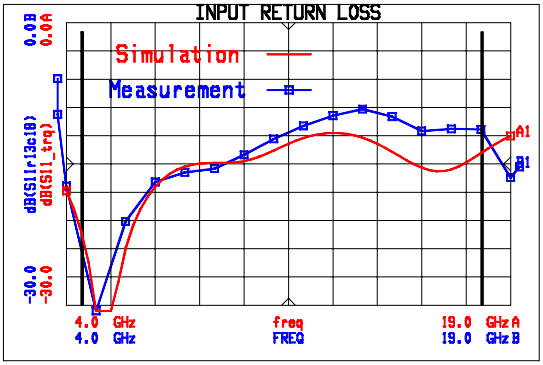

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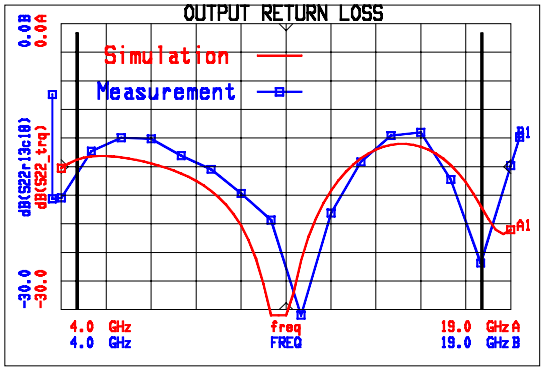

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Figure 2 : Simulated small-signal performances and typical on-wafer measured data

After wafer manufacturing, the circuits were tested for DC operation and RF performances. On-wafer measurements are compared with simulations and show 1 dB less gain. Good agreement is obtained for Input and Output Return Loss. Because of typical breakdown voltage of 20 V for the process, drain voltage has been set at 8 V. Quiescent bias point was 270 mA that is close to Idss/2.

The chip size is 2.6x 3.5 mm^2.

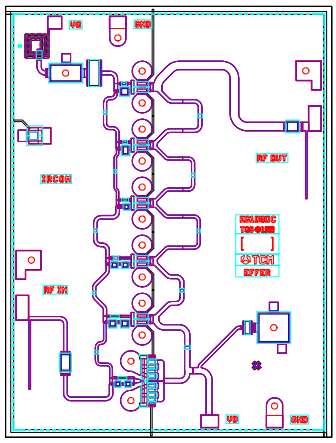


Figure 3 : 1W MMIC Distributed Power Amplifier

On-wafer CW power measurements for Pin=23 dBm, exhibit 28 to 29 dBm output power associated with 5 to 6 dB gain from 4.5 to 18 GHz. Test fixture measurements have been performed. The MMIC circuits were soldered on a Mo carrier and interfaced to the RF connectors with 13mm long 50 Ω microstrip alumina lines. The output power for CW operation at 2 dB gain compression, Vd=9 V and Idq0 was close to 1 W : 830 mW to 1 W from 4 to 18 GHz bandwidth. Figure 4 shows good agreement between predicted and measured output power.

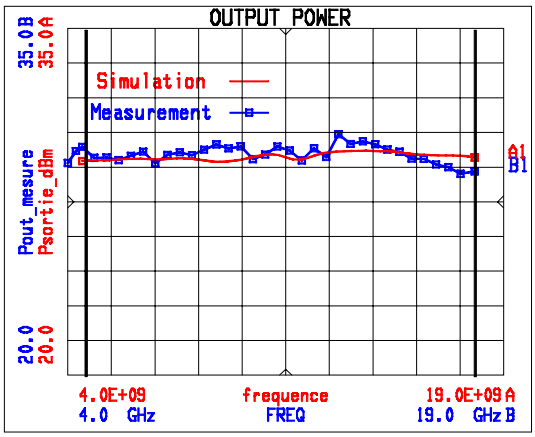


Figure 4 : 1W Class Amplifier, CW output power simulation and test jig measurements (Pin=23dBm, Vds=9 V)

The simulation was performed using non-linear models developed at Ircom with a pulsed measurement system [4]. Also PAE could be simulated and Figure 5 shows more than 20% for the major part of the bandwidth.

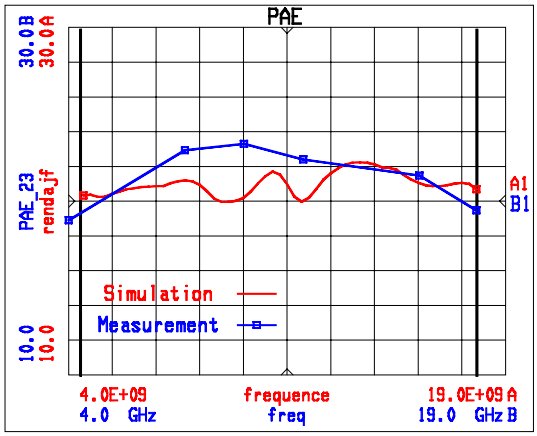


Figure 5 : 1W Class Amplifier, PAE @ Pin=23dBm, Vd=9V, CW operation

B. 2 Watt Class Three Stage power Amplifier

The second topology evaluated is a 3 stage power amplifier (Figure 6). The two last stages are matched for optimum output power based on Load-Pull data provided by TriQuint. The FET used in this circuit is the standard foundry 1200µm pHemt that is fully characterised.

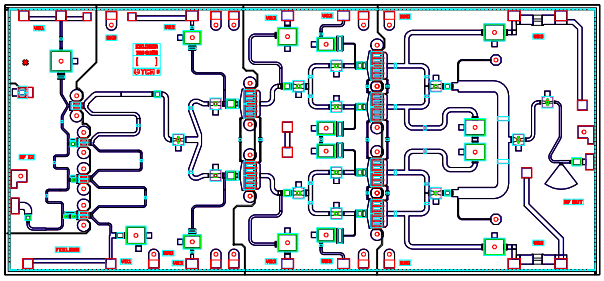
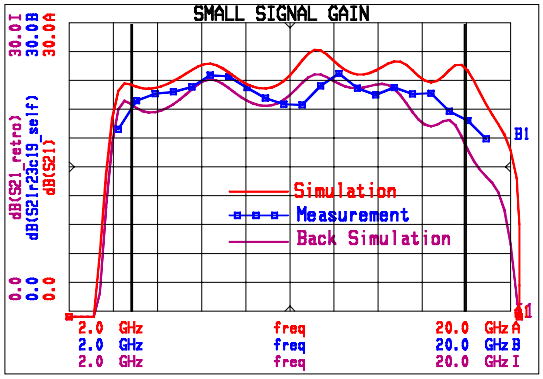


Figure 6 : 2W Class MMIC Power Amplifier layout

The chip is 7.5 x 3.5 mm^2. The first distributed stage has been optimised for gain slope reduction and wide band input return loss. The real difficulty in this structure is the first inter-stage matching network that may introduce parasitic gain ripple over the bandwidth. Figure 7 shows measured and simulated small signal parameters at 8V, Idq0 = Idss/2. Measured gain is 1.5 dB less than simulation. Back-simulation demonstrates that this was inherent to the Fet model. Back-simulated results take also into account EM simulation for the output filter. Gain ripple over the bandwidth has been interpreted and should be corrected for a next iteration.



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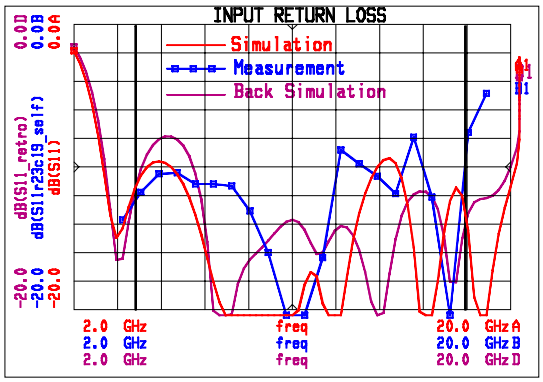

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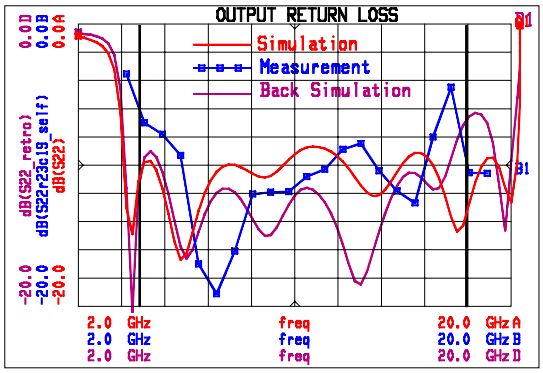

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Figure 7 : [S] parameters for the 2W power amplifier simulations Vs measurements
Vds = 8V, Idss/2

Circuits have been mounted into a test fixture and power measurements have been carried out. Typical CW power performance for 13 dBm input power are shown on Figure 8. This corresponds to 2 or 3 dB gain compression.

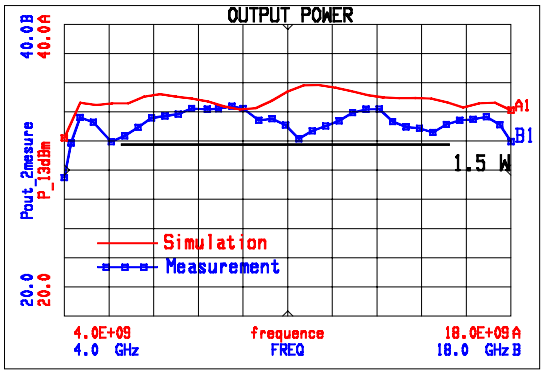

Figure 8 : 2 W Class Amplifier, CW output power simulation and test jig measurements (Pin=13dBm, Vds=8 V)

Simulated output power is about 2dB more than measurement. This is related to the non-linear model which was known to be optimistic, and also to the uncorrected measurement for test fixture losses.

Non linear model has also permitted to simulate the Power Added Efficiency. PAE of 17% to 30% has been measured for typical 25% simulated.

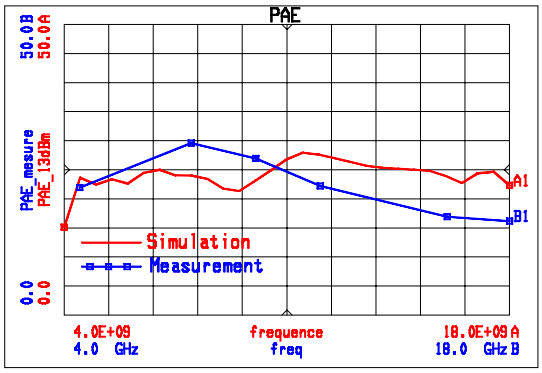

Figure 9 : 2 W Class Amplifier, PAE @ Pin=13dBm, Vd=8V, CW operation

III. CONCLUSION

A first run of wide band power amplifiers has been designed, manufactured and tested. Good results have been obtained. Two octave band [4.5-18 GHz] operation has been reached. The six non-uniform cells 1W distributed amplifier illustrates the methodology for optimum power matching of the structure. Most classical topology with the 3 stage power amplifier has provided near 2 W CW output power with 20dB associated gain. This first iteration has demonstrated that the commercially available pHemt process from TriQuint, Texas is completely suitable for wideband power applications such as EW. A second iteration for the 3 stage power amplifier will be realized and it should overcome gain ripple and chip size.

IV. REFERENCES

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