

A highly integrated MMIC Chipset for 40 GHz MVDS Applications

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Abstract – This paper is intended to give an insight in the development of PHEMT multifunction MMICs (MFC) in the millimetre wave frequency range. It applies to the fast growing Multipoint Video Distribution System (MVDS) market, offering a five-chip solution for the subscriber transceivers. The focus is on the local oscillator, the up-converter and the down converters at 40GHz. These two last chips include a balanced mixer, a buffer amplifier for the local oscillator and a low noise amplifier used either as a LNA (for Rx) or as a transmit driver (for Tx). The design was oriented toward low chip-size in order to reach the cost requirement for such systems. Results are shown from a demonstrator assembly built with these five MMICs.

I. INTRODUCTION

The availability of millimetre-wave short haul communication systems opens the door to a low-cost and truly broadband wireless access to interactive multimedia services (telephone, video, computer data), targeting residential family entertainment as well as business operations. In western Europe, the so-called MVDS system (Multipoint Video distribution System) is actively developed for this purpose, and will be operated in the 40.5-42.5 GHz or 40.5-43.5 GHz frequency band.

In order to address the consumer market, extremely low prices for the millimetre-wave front-end of the subscriber terminals are requested, and, in our view, this will be feasible only with a highly integrated and full MMIC solution, which will drastically simplify the assembly of the front-end module and reduce its cost.

In this paper, we present the performances of a 42GHz MMIC chipset developed for a MVDS transceiver module. With this chipset, the millimetre-wave front-end of a transceiver module can be easily built, using only the five MMICs of this chipset; it is described in the next section.

II. CHIP-SET DESCRIPTION

A. Description of the 40GHz MVDS MMIC chipset

The block diagram of the MVDS transceiver front-end is given in figure 1.

It is composed of a local oscillator, a receiver and a transmitter (for the return path). This transceiver has been designed to use the MVDS 40.5-42.5GHz frequency band and to be fully compatible with the DTH (Direct-To-Home) standard format for the satellite digital TV broadcast, using the same 0.95-2.15GHz intermediate frequency (IF) band.

A full MMIC solution has been retained, and four complex multifunction MMICs have been designed:

- a local oscillator MMIC, including a 10GHz DRO and two cascaded multipliers;
- a receiver MMIC, including a LNA and a down-converter mixer ;
- an transmitter MMIC, including an up-converter mixer and a driver amplifier ;
- an amplifier (DRIV40) for power transmission.

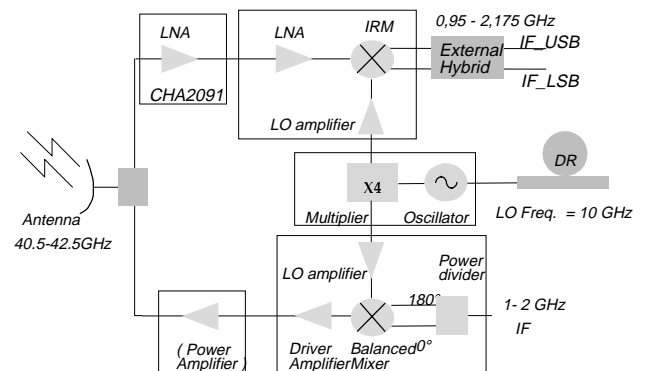


Fig.1 : Block diagram of the transceiver of the MVDS subscriber terminal

All the four MMICs and the CHA2091 (used as the first stage in the receiver path) use UMS pseudomorphic HEMT MMIC process (PH25) with $0.25\mu\text{m}$ Al gates, dedicated to very low-noise and small/medium power circuits up to 40GHz. The typical noise figure of PH25 transistors is 1.5dB with 8dB of associated gain at 40GHz.

The photograph of the demonstrator assembly is given in figure 2. The purpose of this assembly is to demonstrate the functionality of the MMICs and not at all to make a real radio for MVDS. The local oscillator (LO) is placed in the left cavity with an external resonator while the RF input (top) and RF output (bottom) are available on the right hand. For the receiver, we use an external SMD broadband quadrature coupler.

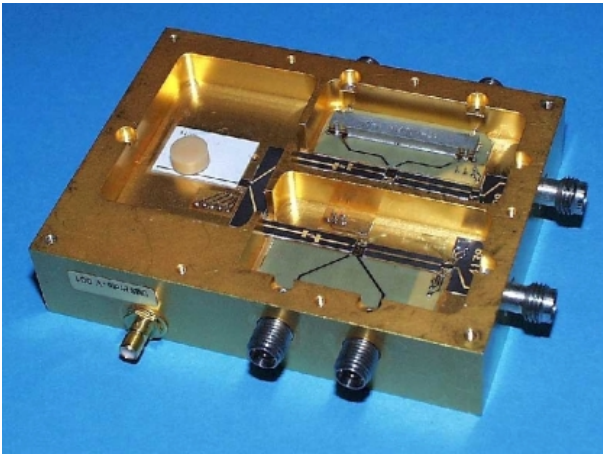


Fig.2 : Photograph of the MVDS transceiver demonstrator at 40GHz.

B. Local oscillator MMIC

This MMIC integrates an X-band DRO and a cascade of two frequency multipliers by 2 as described by the schematic of the figure 3.

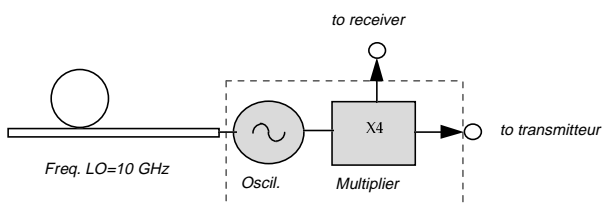


Fig.3 : Principle of the local oscillator

The layout of this oscillator is presented in figure 4.

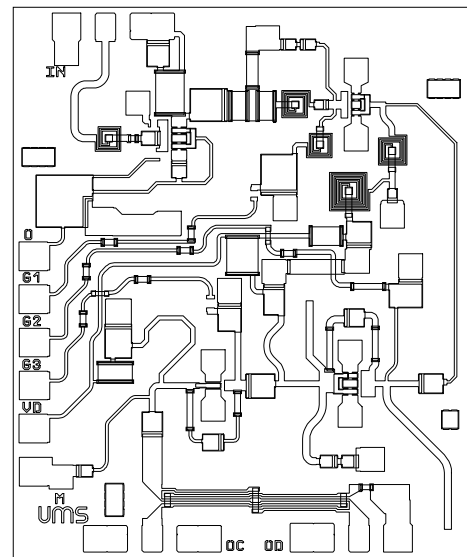


Fig.4 : Layout of the local oscillator. The chip size is 3.4mm^2

The oscillator circuit is stabilised by an off-chip dielectric resonator. It can be adjusted from 9.75GHz to 10.25GHz. After frequency multiplication, this circuit provides 11dBm of power in the LO frequency band 39.5-40.5GHz.

The rejection at the first sub-harmonic at 20 GHz is higher than 30dBc and the rejection of the second harmonic is higher than 16dBc.

The output signal is split in two ways in order to feed the up- and down-converter circuits by an on-chip Lange coupler providing +8dBm for each port. The phase noise measured at 100kHz from carrier at 39.5GHz is 100dBc/Hz.

C. Receiver circuits

The receiver path is composed by two MMIC circuits.

The first one is a MFC down-converter which integrates a 40GHz LNA, a 40GHz local oscillator buffer amplifier and an image rejection mixer (IRM). The schematic is resumed by the figure 5.

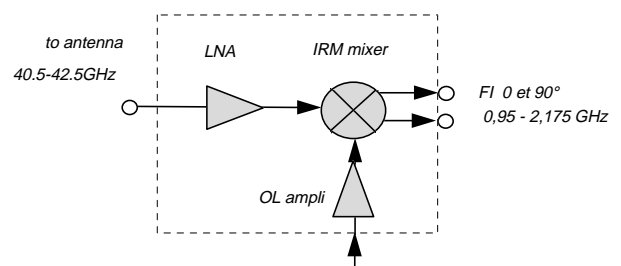


Fig.5 : Principle of the receiver down-converter

The mixer is based on cold FETs structures. The benefit is to not need any drain voltage supply and so to simplify the DC supply design.

To realise a SSB mixer, only two individual cells balanced in quadrature are requested.

The in-phase and 90° RF signals are obtained using a Lange coupler and the IF signals must be recombined off-chip for image frequency rejection. The layout of this MMIC is displayed in figure 6.

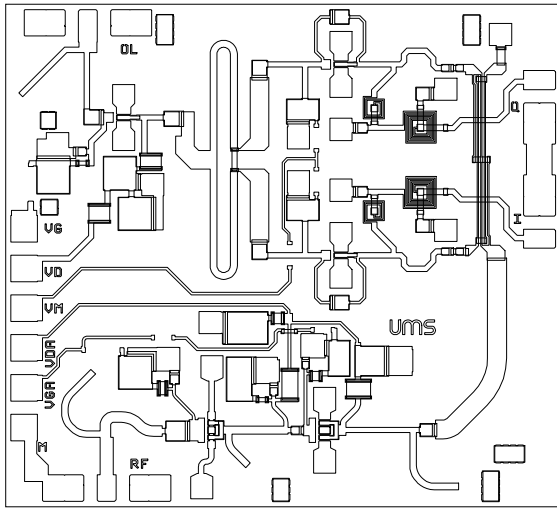


Fig.6 : Layout of the down-converter MFC. The chip size is 4.3mm²

The second MMIC circuit is the UMS catalogue product low noise amplifier CHA2091 (figure 7).

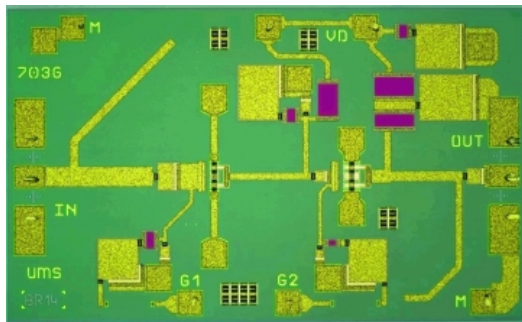


Fig.7: Photograph of the LNA CHA2091

This two-stage amplifier exhibits a 14dB gain and a 3.0dB noise figure in the 36 to 40 GHz frequency band. The use of this amplifier can be extended up to 43GHz, and so be used for these applications.

The overall measured receiver path conversion gain is higher than 20dB in Upper Side Band (USB), and the image frequency rejection is better than 20dBc. The results in Lower Side Band (LSB) are almost the same but the slope is different due to a different combination

of the frequency slope of the IF filter, of the RF one and of the CHA2091 itself. The overall Noise Figure is lower than 4.0dB, accounting for a 1.0dB degradation brought back by the MFC down-converter (compared to the 3.0dB of the CHA2091 itself).

The LO buffer amplifier of the MFC is useful to isolate the mixer from the external (assembly) and also to reduce the required power for the LO (typically 0dBm) that may radiate from the bonding wire. This feature is very important to reduce the level of the spurious in the radio, as the specifications are more and more demanding on these aspects.

Two accesses are provided for the IF in order to use the IF external quadrature combiner for the image suppression.

The conversion gain and image rejection results shown in figure 8 include all the effects of the assembly and external hybrid combiner (shown in figure 2).

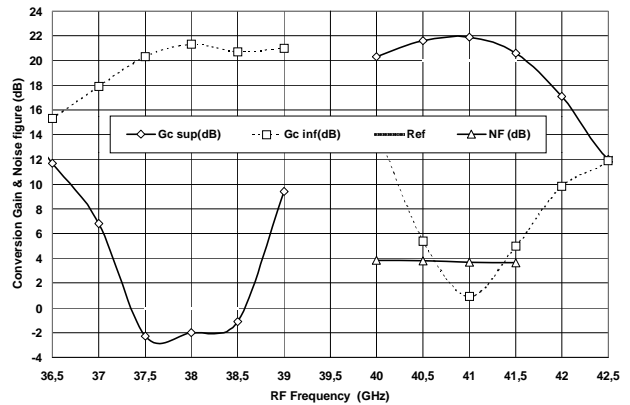


Fig.8: Full Hybrid measurement: Conversion Gain (USB & LSB), Image Rejection and Noise Figure

D. Transmitter circuits

The transmitter path is composed also by two MMIC circuits.

The first one is a MFC up-converter which integrates a LO buffer amplifier, an IF input splitter circuit, a balanced mixer for LO rejection, and a two-stage driver amplifier. These four parts are described by the schematic of the figure 9 below.

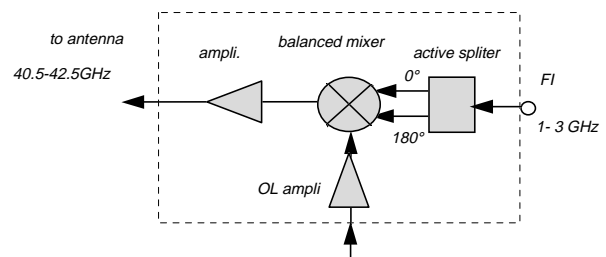


Fig.9: Principle of the receiver up-converter

The layout of this MMIC is displayed below in figure 10.

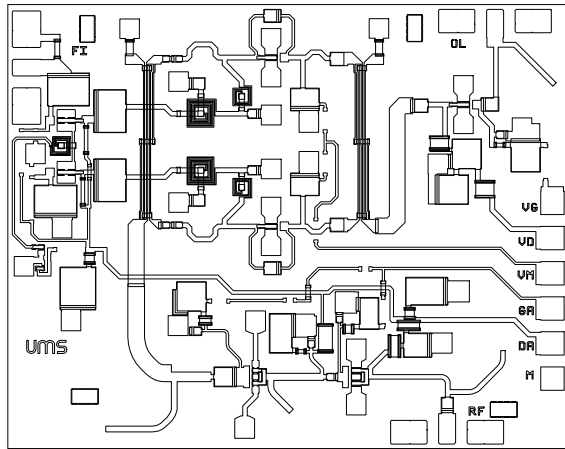
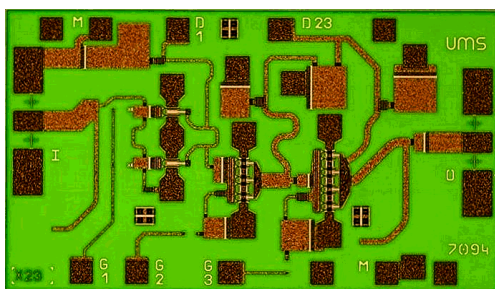


Fig.10: Layout of the up-converter MFC. The chip size is 4.9mm²

The balanced mixer is composed of two cold FETs biased at pinch-off and placed between two Lange couplers to split the LO signal, recombine the RF signal and reject the LO signal on the output port. The input splitter circuit provides the mixer with the in phase and inverted IF signals.

The second MMIC circuit is the medium power amplifier described by the photograph of the figure 11. It provides the transmitted power of the return path signal. It is a three-stage amplifier: the gain is higher than 16dB with an output 1dB compression point about 16-17dBm.



DRIV40

Fig.11: Photograph of the transmitter medium power amplifier

The overall conversion gain is better than 20dB up to 3GHz IF and the LO to RF isolation at the RF port is better than 20dBc for -20.0dBm IF input power. The Pout for 1dB gain compression is achieved for an IF input power of -6dBm at an RF frequency equal to 43GHz. The figures 12 and 13 show the behaviour of

this circuit respectively in the frequency band and for the non-linear performances.

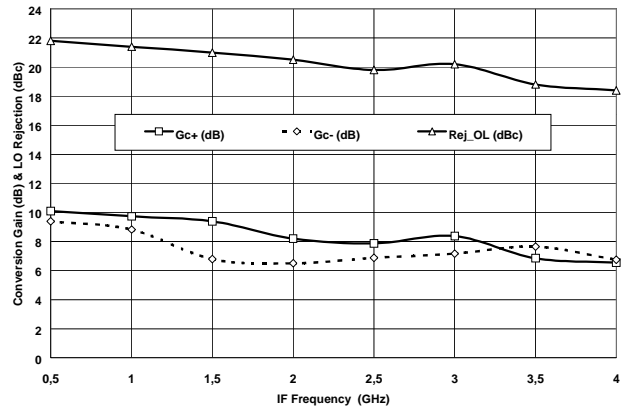


Fig.12: Full Hybrid Measurement: Up-Converter conversion gain and LO suppression

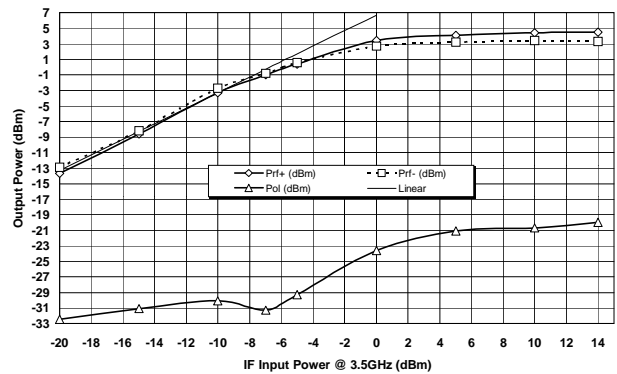


Fig.13: Full Hybrid Measurement: Up-Converter Pin/Pout and LO leakage @ 43 GHz RF

III. CONCLUSION

We have successfully demonstrated the development of a chipset including three complex 40GHz multifunction MMICs, providing a full MMIC solution for the fabrication of a transceiver module of a MVDS subscriber terminal.

ACKNOWLEDGEMENTS

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