

GaAs MIXED SIGNAL MULTI-FUNCTION X-BAND MMIC WITH 7 BIT PHASE AND AMPLITUDE CONTROL AND INTEGRATED SERIAL TO PARALLEL CONVERTER

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Abstract - The design and measured performance of a GaAs multi-function X-band MMIC for space-based synthetic aperture radar (SAR) applications with 7-bit phase and amplitude control and integrated serial to parallel converter (including level conversion) is presented. The main application for the multi-function chip (MFC) is to provide full amplitude and phase control in the transmit path and the receive path of T/R modules. The MFC has been realised in the OMMIC ED02AH 0.2 μm PHEMT process providing enhancement and depletion FET's.

I. INTRODUCTION

In phased array radars and synthetic aperture radars (SAR), the demand for small size circuits with low power consumption is growing. The performance and costs of these circuits must be attractive. By using microwave monolithic integrated circuits, these demands can often be met. Phased array radars use up to thousands of antenna elements all driven by transmit/receive (T/R) modules containing several functions. The volume available for these T/R modules is very limited, considering $\lambda/2$ element spacing and the trend toward smart skins. The demand for size reduction of the transmit/receive modules or even integration of antenna and transmit/receive modules becomes more and more important. By integrating several functions such as phase and gain control, low-noise and driver amplifiers and T/R switches on a single multi-function chip, the size of a transmit/receive module can be considerably reduced.

Higher integration implies a large number of control lines to the chip. In the case of a parallel controllable multifunction chip [1] with 7-bit phase and amplitude control and T/R switches, the number of control lines can be up to 32. Half of the control lines are inverted signal levels. By integrating a serial to parallel converter on-chip, the number of control lines can be substantially reduced. From T/R module point of view, further advantages are: less bonding wires, no off-chip level converters or inverters are needed and the number of pins of the control ASIC can be reduced. The multi-function X-band MMIC described in this article can be serially

controlled. Only three control lines are needed to set a 7-bit phase shifter, 7-bit attenuator and input and output T/R switches. The MFC is optimised to have an acceptable noise figure, a good third order intercept point, sufficient output power to drive a high-gain power amplifier, low power dissipation and a small chip area. This MFC is designed for a space-based SAR application but is also very suitable for phased array radars.

II. DESIGN TOPOLOGY

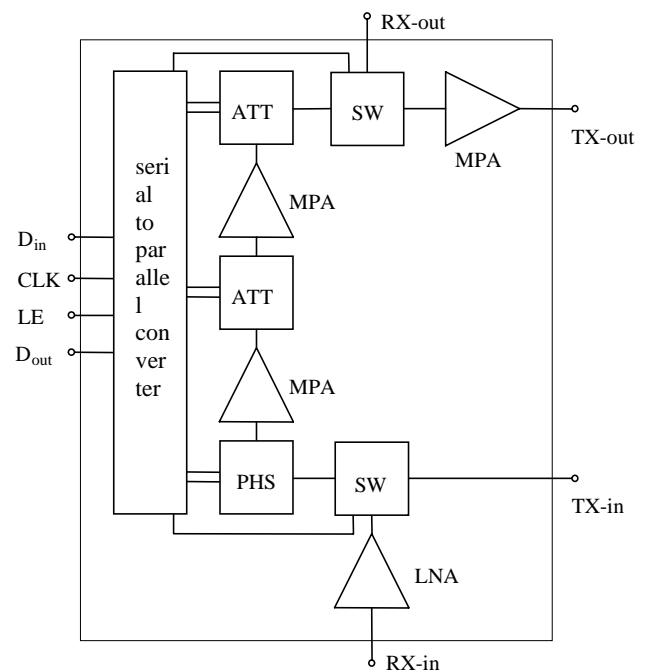


Figure 1: Block diagram of the GaAs multi-function MMIC.

A block diagram of the MFC is shown in figure 1. The MFC consists of an input and output switch (SW) for switching between transmit and receive mode, a low noise amplifier (LNA) for the receive chain, a common path and a driver amplifier (MPA) for the transmit chain. The common path of the MFC consists of a 7-bit phase shifter (PHS), two interstage amplifiers and a 7-bit attenuator (ATT). The used circuit topology is based on a trade-off between noise figure, third-order intercept

point, 1dB compression point, insertion gain and power-dissipation. To meet all the MFC requirements, a low-noise amplifier is placed at the input of the receive chain and a driver amplifier is placed at the output of the transmit chain of the chip. Hence, both amplifiers are placed outside the common path. One amplifier inside the common path is placed between the phase shifter and attenuator to minimise interaction. To minimise power dissipation, the LNA is switched off in the transmit mode and the driver amplifier is switched off in the receive mode. In this way only three amplifiers are used in both modes. A photograph of the GaAs multi-function X-band MMIC is shown in figure 2. The MFC has only 13 bonding pads on the left side of the chip. This is considerable less compared with a parallel controlled MFC.

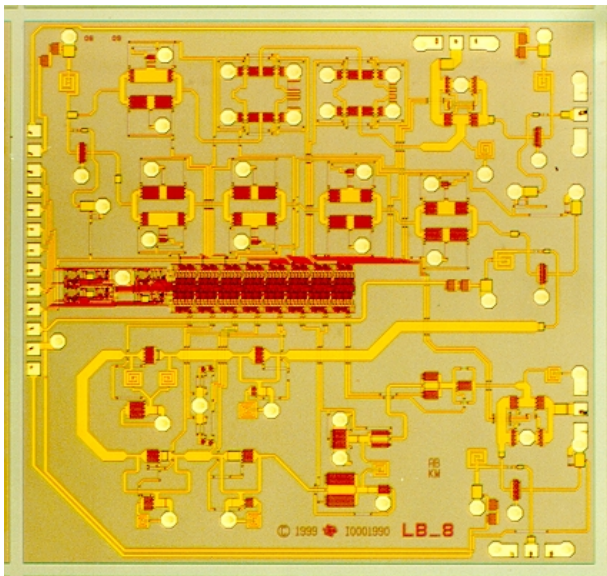


Figure 2: Photograph of the GaAs multi-function X-band MMIC for SAR applications ($4.2 \times 4.4 \text{ mm}^2$).

III. SERIAL TO PARALLEL CONVERTER

As mentioned before, in order to improve further integration, a 16-bit serial to parallel converter is added to the MFC in order to control the 7-bit phase shifter, 7-bit attenuator and the input and output T/R switch. The serial to parallel converter can be seen in the middle of the photograph shown in figure 2. The digital circuitry consists of 16 shift registers and some additional circuitry to generate the clock and perform the conversion from external TTL/CMOS level to the internal Direct Coupled Fet Logic (DCFL) which is used on-chip. A functional block diagram is given in figure 3. Each shift register contains 3 D flip-flops and a driver which is used to drive the RF switches. Both complementary switching voltages (0 V and -1.5 V) are available at the output of the driver. The layout of the shift register is designed in such a way that it is easy cascadable. Therefore, it can be adopted for designs with an arbitrary number of bits.

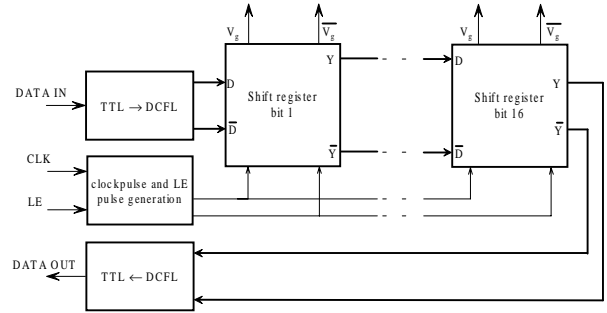


Figure 3: Functional block diagram of the digital on-chip circuitry.

Supply voltages of +5V, +2.5V and -5V are needed for the digital circuitry. The total power consumption for 16 shift registers and the necessary additional on-chip circuitry is less than 70mW. The power consumption of the total chip, digital circuitry included, is less than 0.6 W. During measurements, a serial bit stream was clocked into the digital circuitry (DATA IN) using a standard personal computer. The DATA OUT bit stream is available on-chip and can be fed to a second chip or it can be used for testing purposes. The digital drivers have been tested with a clock speed of 100 kHz but are expected to work with a clock speed up to 20 MHz. A photograph of a part of the chip with the integrated serial to parallel converter is shown in figure 4. The used chip area of the serial to parallel converter is about 0.74 mm^2 . The saved chip area by removing the large number of bonding pads in the case of a parallel controllable chip is about 0.43 mm^2 . So, the increase of chip area is only 0.31 mm^2 .

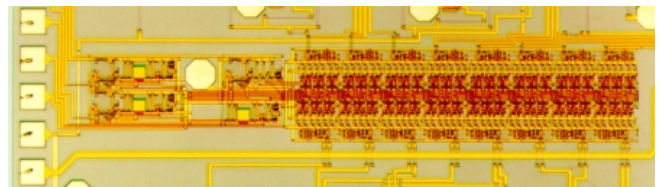


Figure 4: Photograph of the integrated 16-bit serial to parallel converter (area: 0.74 mm^2).

IV. MEASUREMENT RESULTS

The measurement results of the MFC are shown in this section. There are seven bits cascaded for the phase shifter and attenuator but only a 6-bit resolution is required for the application. Most of the measurement results shown in this section are presented for the selected number of states. In figure 5 the maximum and rms phase error versus frequency in the receive mode is shown. The values are obtained over all the selected phase states. The maximum phase error is about $\pm 3^\circ$ and the calculated rms error is even less than 1.5° . In figure 6 the gain, input and output return losses versus frequency in the receive mode are shown. The results are the maximum values over all the selected phase states (representing the worst-case situation).

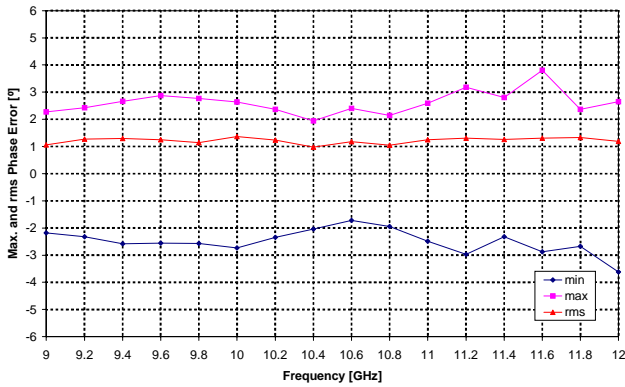


Figure 5: The measured maximum and rms phase error versus frequency of the MFC in the receive mode. The values are obtained over all the selected phase states.

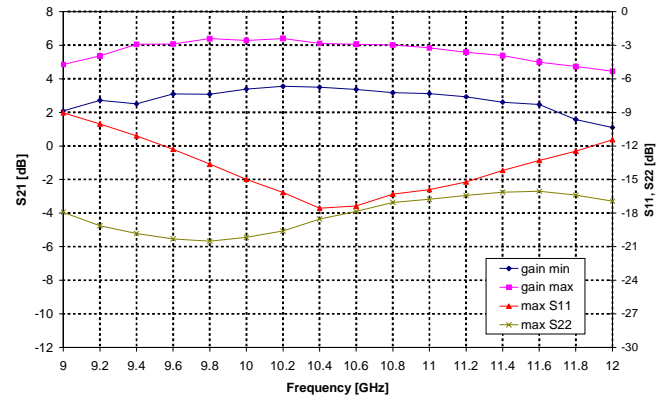


Figure 6: The measured gain, input and output return losses versus frequency of the MFC in the receive mode. The values are the maximum (or minimum) obtained over all the selected phase states.

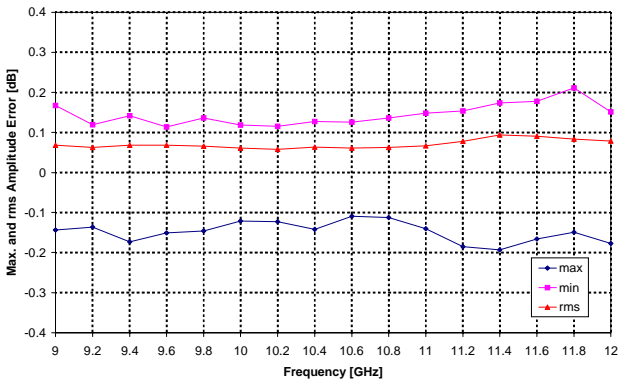


Figure 7: The measured maximum and rms amplitude error versus frequency of the MFC in the receive mode. The values are obtained over the selected gain states.

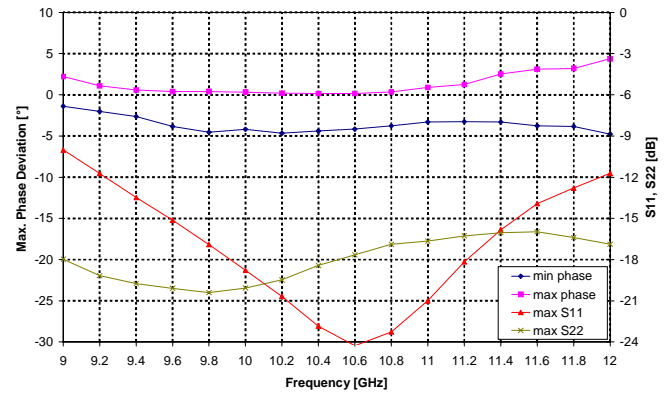


Figure 8: The measured phase variation, input and output return losses versus frequency of the MFC in the receive mode. The values are the maximum (or minimum) obtained over all the selected gain states.

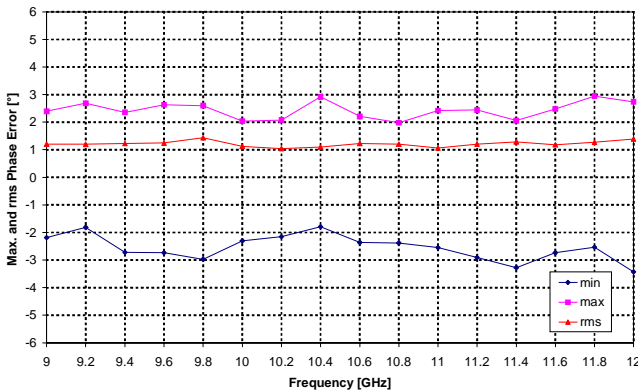


Figure 9: The measured maximum and rms phase error versus frequency of the MFC in the transmit mode. The values are obtained over all the selected phase states.

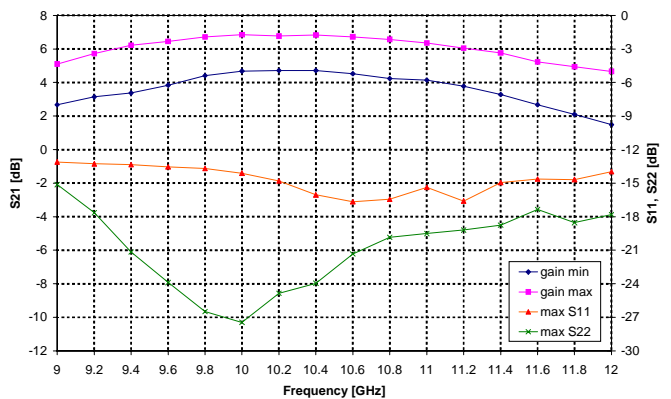


Figure 10: The measured gain, input and output return losses versus frequency of the MFC in the transmit mode. The values are the maximum (or minimum) obtained over all the selected phase states.

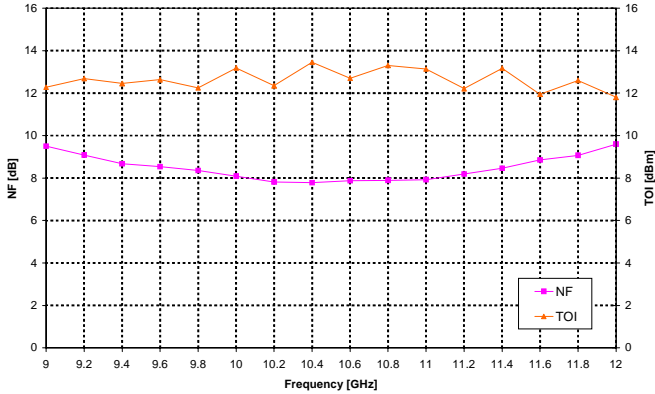


Figure 11: The measured noise figure and third order intercept point versus frequency of the MFC in the receive mode. These measurements are performed in the reference state (maximum gain).

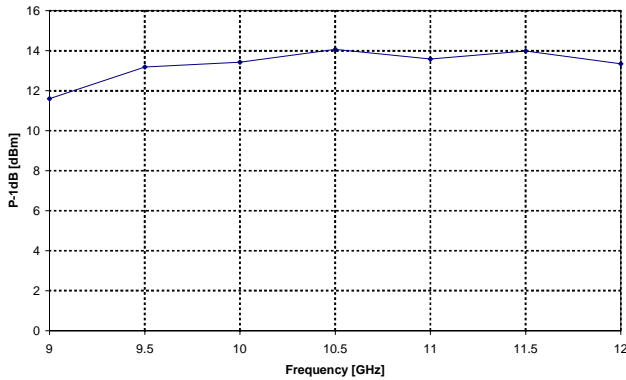


Figure 12: The measured P_{-1dB} compression point versus frequency of the MFC in the transmit mode. This measurement is performed in the reference state (maximum gain).

From figure 6 a maximum PM to AM conversion of 3 dB can be observed. The input return loss varies between 9 and 17 dB over the frequency band and the output return loss is better than 16 dB. In figure 7 the maximum and rms amplitude error versus frequency in the receive mode is shown. The values are obtained over the selected gain states. The maximum amplitude error is about ± 0.15 dB. The calculated rms amplitude error is about 0.08 dB. In figure 8 the phase variation, the input and output return losses versus frequency for the receive mode are shown. The values shown are the maximum or minimum over the selected gain states. From the figure it can be seen that the maximum phase variation is about 5° for the lower frequencies and about 10° for the higher frequencies.

In figure 9 the maximum and rms phase error versus frequency in the transmit mode is shown. The values are obtained over all the selected phase states. The maximum phase error is about $\pm 3^\circ$ and the calculated rms error is even less than 1.5° . In figure 10 the gain, input

and output return losses versus frequency in the transmit mode are shown. The results shown are the maximum values over all the selected phase states. The input return loss in the transmit mode is better than 12 dB and the output return loss is better than 15 dB. In figure 11 the measured noise figure and the third order intercept point at the output versus frequency in the receive mode are shown. These measurements are performed at the reference state (max. gain). From the figure it can be seen that the noise figure is less than 10 dB with a minimum of 8 dB. The third order intercept point at the output is better than 12 dBm. The measured P_{-1dB} compression point versus frequency in the transmit mode is shown in figure 12. This measurement is performed at maximum gain. From the figure it can be seen that the maximum P_{-1dB} output power is 14 dBm.

V. CONCLUSIONS

The integration of phase and amplitude functions combined with a serial to parallel converter on-chip is presented in this paper. The MFC is easy to control and it has good specifications. This makes this multi-function chip extremely suitable for high performance space-based synthetic aperture and phased array radars.

In summary, the frequency range is from 9 to 12 GHz for both transmit and receive. The phase setting of the MFC is from 0° to 360° with an accuracy better than $\pm 3^\circ$. The rms phase error is less than 1.5° . The gain setting range is 20 dB with an accuracy better than ± 0.2 dB. The rms amplitude error is about 0.08 dB. The gain for transmit and receive is about 5 dB. The noise figure for the receive chain is better than 10 dB with a third order intercept point of 12 dBm. The maximum P_{-1dB} compression point of the transmit chain is about 14 dBm. The total power consumption of the chip, digital circuit included, is less than 0.6 Watt and the size of the MFC is $4.2 \times 4.4 \text{ mm}^2$.

In combination with a low noise amplifier and a high gain power amplifier it is possible to make a three chip T/R module solution.

VI. ACKNOWLEDGEMENT

The contribution from our colleague P.C. de Jong for the design of the digital unit cells was highly appreciated.

VII. REFERENCES

- [1] A. de Boer, M.W. van der Graaf, A.P. de Hek, T.C.B. Tieman, *A GaAs multi-function X-band MMIC for space-based SAR application with 7 bit phase and amplitude control*, GAAS 98, pp. 215-220, October 1998.