High Power silicon
MMIC design for wireless base stations

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Abstract: This article presents the specificities of high power silicon MMIC , intended for wireless base station applications. Motorola's LDMOS technology , and its integrated version (HVIC) , are presented , with emphasis on the particularities of high power functions .The technical problems linked to the design of multistages power amplifiers, of 10W and 30W output power are listed, and solutions are proposed. Two power amplifier circuits , a 900 MHz 3stages 30W and a 1800MHz 3 stages 10W and their associated performances demonstrate the validity of these solutions.

I.TECHNOLOGY

When it comes to power amplification for wireless base station, LDMOS is the technology of choice. Indeed, the supply voltage (26V) and the power levels of interest (a few watts to several hundreds)lead to electrical constraints (such as breakdown voltages) and thermal constraints (very low thermal resistances) that GaAs devices have a hard time to reach. LDMOS is a silicon MOSFET technology with the following properties:
-breakdown voltages in the order of 70V
-0.6 microns gate length .
-thermal resitances as low as a few tenth of degrees/W.
In consequence LDMOS is a transistor technology perfectly suited for power amplification up to 150W at 1 and 2 GHz.
The association of passive components on Silicium has triggered the design of multistage power amplifiers.

The microstrip transmission lines and the inductances are the limiting components because of their very low quality coefficient, in the order of 5 to 6, for frequencies between 1 and 2 GHz. The coupling by proximity to the low resistivity substrate is responsible for this single digit Q.

II.SPECIFIC PROBLEMS

Reaching power levels in the order of 10 to 15W requires transistors with a gate periphery of 30mm to 40mm , 30W corresponds to an 80mm device. These devices feature RF gate and drain impedances around 1 or 2 ohms. Their physical size ranges between 2000 and 5000 microns in the Y-axis and 200 microns in the X-axis.
The reactive elements used for impedance matching purposes exhibit much smaller dimensions , around 100 microns. In addition to that , the line width for transmission lines and inductances (and then the connection width) varies between 5 and 30 microns.

This creates several problems:

-The matching loss are prohibitive because of the low Q of the transmission lines and inductances on one hand, and the very low impedances of the transistors on the other hand.

-The major size difference between actives and passives makes impossible the in phase excitation of the transistor fingers. This is incompatible with power generation at the output of the transistor.

-Inaccurate simulations result because of the excessive scaling ratio.

III.PROPOSED SOLUTIONS

Several techniques allow the designer to get around , or at least attenuate the above mentionned problems. Shrinking the gate periphery of the individual transistors , and combining them in a branched amplifier structure represents the key to success. The following advantages result :

-Matching loss major decrease because of two reasons:
*Transistor impedance level increase
*matching networks duplication.

-Output power increase because of a better in phase excitation of the different fingers, due to the aspect ratio difference reduction between passives and actives.

-Thermal resistance improvement, or MTTF increase , because of the transistor splits.

There is a possibility to optimize a little bit further by increasing the unit finger width , which reduces further the size difference (in the Y-axis) between actives and passives and then improves the in phase excitation.

IV.PRACTICAL EXAMPLES

The above presented techniques have allowed 2 circuits design :
-A 3 stages amplifier , in the 1.805GHz-1.880GHz band, featuring 15W 1dB compression point. The line-up is based on a 5mm fet driving a 10mm fet driving two 20mm fets.
-A 3 stages amplifier , in the 925MHz-960MHz band , featuring 30W compression point and using a 5mm fet to drive two 5mm fets , driving four 20mm fets.

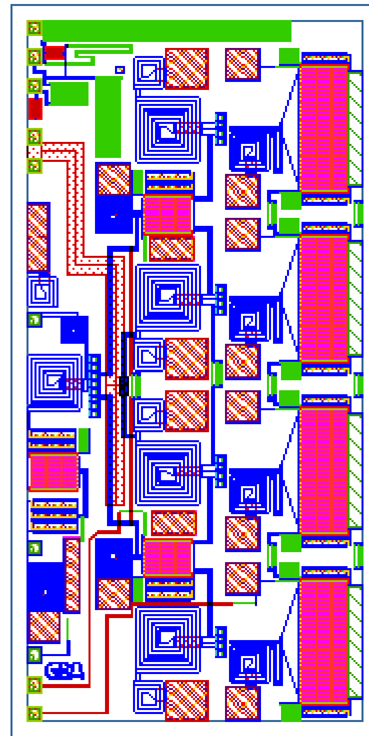

Fig1: 30W 900MHz amplifier layout.

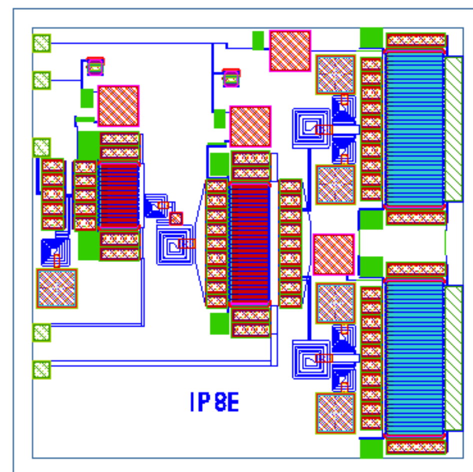

fig 2: 15W 1.8GHz amplifier layout

These two amplifier performances are presented in figures 3 to 6.

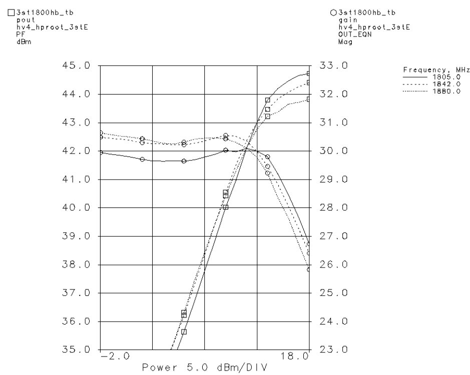

fig3: 1.8GHz amplifier :gain and power

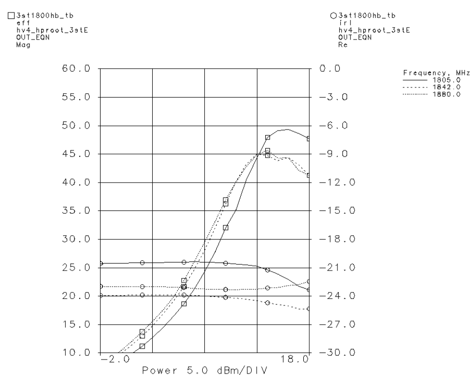

fig4 : 1.8GHz amplifier : Power Added Efficiency and S11.

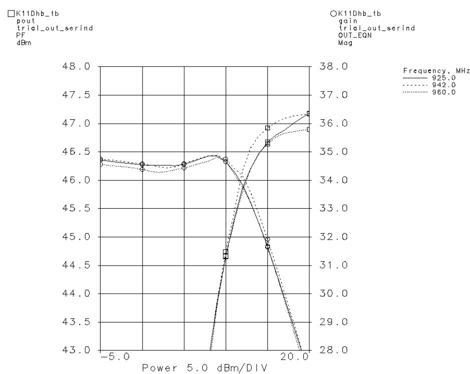

fig 5 : 900MHz amplifier :gain and power

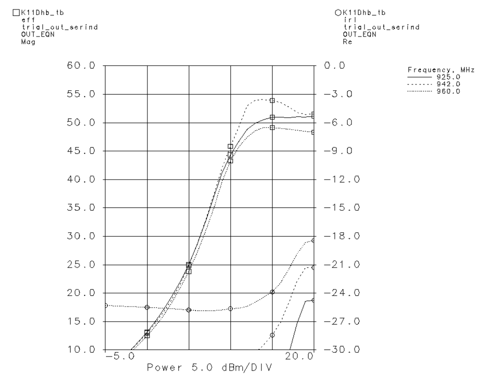

fig 6 : 900 MHz amplifier :PAE and S11.

V.CONCLUSION

The possibility to reach several tens of watts using Silicon MMIC has been demonstrated in this article. Nevertheless, it is necessary to use branched structures amplifiers , using limited gate periphery transistors , along with optimized unit finger width. In addition to the electrical advantages , or simply to the possibility to realize a circuit , these techniques lead to thermal improvements.

It is mandatory for the designer to pay a specific attention to the stability analysis , mainly because of the presence of loops .To that extent the Normalized Determinant Factor technique represents the perfect tool.