

Noise performance of a ground gate wideband MMIC amplifier

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Abstract-A broadband ground gate amplifier was designed, fabricated and characterized. Noise parameters of the intrinsic HFETs were measured and simulated by using Pospieszalski noise model. Extracted drain and gate temperatures were used for the characterization of the amplifier noise properties. An input match better than -20 dB in a wide band from 2 to 6 GHz and -10 dB from 1-13 GHz with corresponding 11 dB gain was obtained. NF_{min} of 3 dB was found experimentally at room temperature. A dc power dissipation of less than 20 mW is possible to obtain with this device technology. The total chip area is $2 \times 1.5 \text{ mm}^2$. The active circuit area is less than 1 mm^2 . We have simulated amplifiers rf and noise performance with the wider gate HFET at the input.

I. INTRODUCTION

A broadband MMIC amplifier is intended as an electronically adjustable input resistance IF-amplifier. It is based on a common gate HEMT input stage followed by a common source HEMT. This configuration is typically used as an IF-amplifier in frequency mixers. There is a need for low noise broadband amplifiers for frequency mixers with adjustable input resistance in order to minimize the reflection losses. At present, reflection matched amplifiers are used where state of art low noise characteristics are required, but these have a small bandwidth and their input resistance is not possible to adjust in a simple way. A broader matching condition can be obtained by using a balanced circuit topology at the expense of circuit complexity and doubled power dissipation [1]. In this work we have investigated the amplifier with a common gate HEMT followed by a common source HEMT as a broadband IF-amplifier with an electronically adjustable input resistance.

II. THE CIRCUIT TOPOLOGY

The amplifier was designed to have the gates and drains of both transistors accessible for the dc probes. This enabled the experimental investigation of the bias-noise-gain trade-off. The first transistor has a gate width of $60 \mu\text{m}$ yielding a maximum transconductance of nominally 70 mS. The input resistance of the first stage is electronically adjustable by the gate bias voltage, V_{g1} . This resistance is approximately the inverse of the transconductance. By adjusting the transconductance, the input resistance can be electronically tuned.

For an input resistance of 50Ω , the transconductance should therefore be tuned to 20 mS. The second transistor has a gatewidth of $4 \times 25 \mu\text{m}$ yielding a

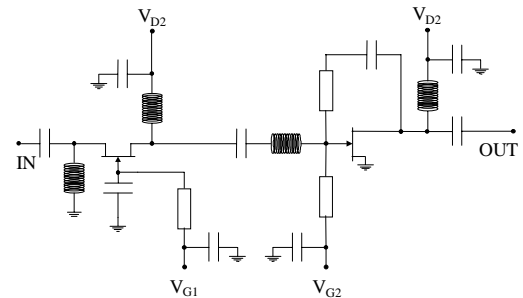


Fig.1 The broadband amplifier circuit diagram.

maximum transconductance of nominally 140 mS. The gain of the second stage is flattened by resistive feedback. An inter-stage inductor is used in order to achieve a flat gain from first stage. The gates are biased through 500Ω gate resistors. The input and output stages are designed as dc-isolated through coupling capacitances.

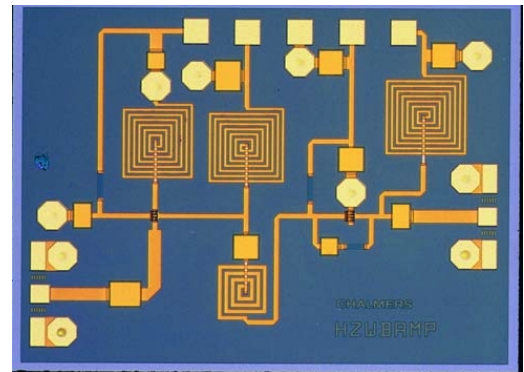


Fig.2 The chip photo of the broadband amplifier.

The layout of the MMIC is shown in fig.2. The total chip area is $2 \times 1.5 \text{ mm}^2$. The active circuit area is less than 1 mm^2 .

III. EXPERIMENTAL RESULTS AND SIMULATIONS

The noise parameters of intrinsic transistor DOPH1 [2] were measured at different bias conditions. The Pospieszalski parameters T_D and T_G [3] were initially extracted (see fig.3) and then tuned by the direct

optimization with gradient method. Once the optimized values were calculated, a nonlinear curve fitting was performed to obtain an analytical expression for both T_G and T_D as a function of the current density. The most accurate

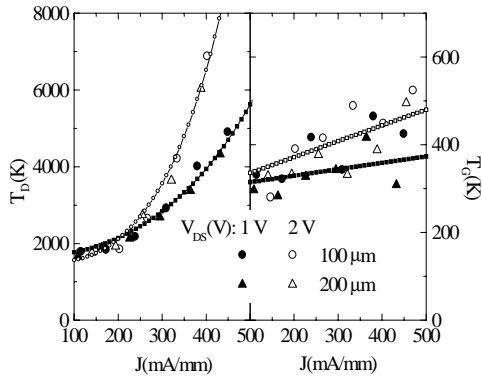


Fig.3 Pospieszalski drain and gate temperatures versus drain current. Solid triangles and circles correspond to optimised T_D and T_G when $V_{D1}=1$ V, open $V_{D1}=2$ V. Lines correspond to the fitted values.

prediction of the noise parameters was achieved by assuming a linear dependence for T_G and a hyperbolic one with a current density offset for T_D ,

$$T_D = T_{D0} \cosh \frac{J_D - J_0}{J_1}$$

where T_D is the drain temperature, T_{D0} , J_0 and J_1 are fitting factors. The accuracy of this expression has been verified at bias points near pinch-off operation [4]. The

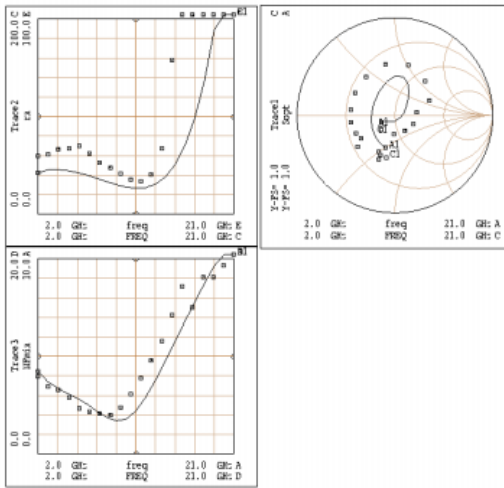


Fig.4 Measured (squares) and simulated R_n (up to the left), NF_{min} and G_{opt} (up to the right) of the grounded gate amplifier. $V_{D1}=0.45$ V, $V_{D2}=1.5$ V, $V_{G1}=-0.006$ V, $V_{G2}=0.45$ V.

extracted and fitted values were used for the simulation of the NF_{min} , R_n and optimum source reflection coefficient.

The MMIC was characterized by a vector network analyzer HP8510C, and an “on wafer” noise parameter measurement system (ATN). The bandwidth of the MMIC amplifier is approximately 13 GHz. Simulated NF_{min} , R_n and G_{opt} versus frequency are presented in the fig.4. An acceptable fit was obtained except some discrepancies for noise resistance. In the fig.5 the simulated and measured s parameters of an amplifier are presented.

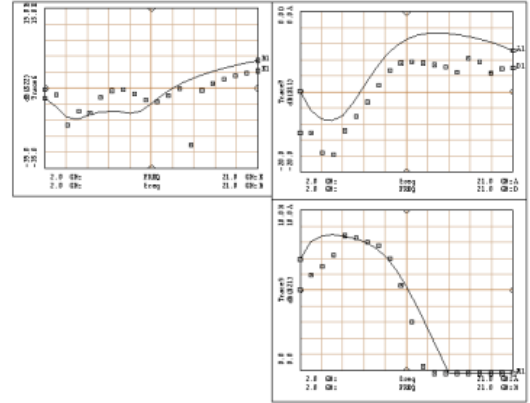


Fig.5 Measured (squares) and simulated s parameters of the grounded gate amplifier versus frequency. s22 (up to the left), s11 (up to the right) and s21. $V_{D1}=0.45$ V, $V_{D2}=1.5$ V, $V_{G1}=-0.006$ V, $V_{G2}=0.45$ V.

The input reflection coefficient was less than -10 dB, output reflection coefficient less than -15 dB in 2-13 GHz frequency range. We have investigated noise and s parameters for the set of drain and gate biases and have found that the best bias corresponds to $V_{D12}=1.5$ V, $V_{G12}=-0.006$ V.

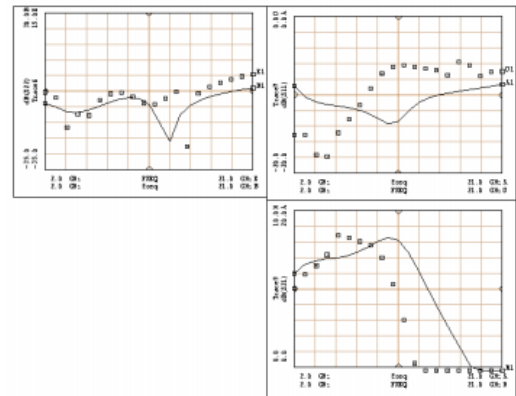


Fig.6 Simulated s parameters of an amplifier biased with $V_{D12}=1.5$ V, $V_{G12}=-0.006$ V (lines) in comparison with measured (open squares) $V_{D1}=0.45$ V, $V_{D2}=1.5$ V, $V_{G1}=-0.006$ V, $V_{G2}=0.45$ V.

In Fig.6 simulated and measured s parameters of an amplifier biased with $V_{D12}=1.5$ V, $V_{G12}=-0.006$ V are presented. We have more flat and less input reflection coefficient and higher s21 (notice different scales in Fig.6, a, c). The noise parameters of an amplifier biased with $V_{D12}=1.5$ V, $V_{G12}=-0.006$ V were simulated using the methodology described above. We see (fig.7) that minimum noise figure of the amplifier is around 4 dB in

a wide band and is improved especially at higher frequencies ($f > 10\text{GHz}$). The noise resistance is lower at high frequencies too. These results show that grounded gate amplifier is a good approach of the broadband amplifier with an adjustable input.

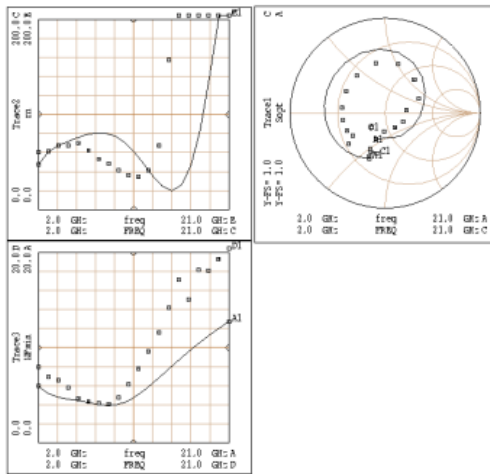


Fig.7 Simulated noise parameters of an amplifier biased with the bias point $V_{D12}=1.5\text{ V}$ $V_{G12}=-0.006\text{ V}$ (lines) in comparison with measured (open squares).

Moreover we have performed simulation of the s and noise parameters with the wider gate ($W=4 \times 25\ \mu\text{m}$) transistor at the input stage instead of $60\ \mu\text{m}$ as well (see fig.8). This was done in order to predict the best noise-gain trade-off.

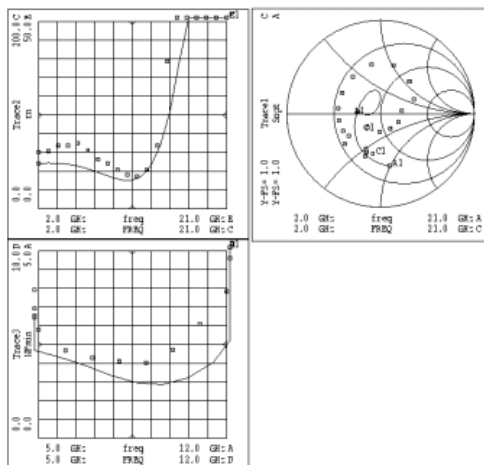


Fig.8 Noise parameters of the amplifier with the wider gate ($W=4 \times 25\ \mu\text{m}$) DO1PH transistor at the input (Trace 1, 2, 3). Open squares correspond to measured and lines to the simulated. Notice different scales, NF_{\min} , 5 dB per scale and R_N 50 Ohm per scale corresponds to the simulated results.

We observe the improvement of the minimum noise figure (less than 1.5 dB at 8 GHz) and 4 times lower noise resistance especially at higher ($f > 10\text{ GHz}$) frequency. The optimum reflection coefficient is close to 1 and less frequency dependent. This means that amplifier is well matched with 50 Ohm system in terms of noise figure. We have simulated s parameters of this approach, see fig. 9. As we expected the NF_{\min} of the amplifier was obtained lower and s_{21} higher due to the

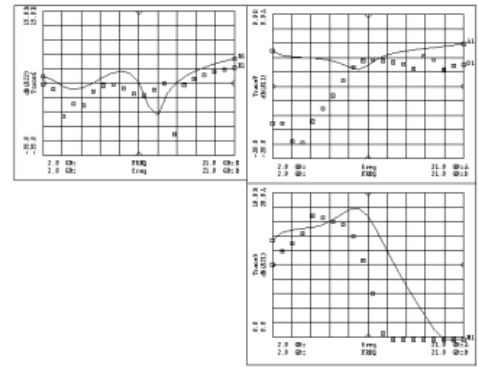


Fig.9 Simulated s parameters (lines) of the amplifier with a wider gate transistor at the input stage in comparison with measured. $V_{D12}=1.5\text{ V}$, $V_{G12}=-0.006\text{ V}$, $T_D=4100\text{ K}$, $T_G=300\text{ K}$ for the simulated and $V_{D1}=0.45\text{ V}$, $V_{D2}=1.5\text{ V}$, $V_{G1}=-0.006\text{ V}$, $V_{G2}=0.45\text{ V}$ for the measured. Notice different scale for the s_{21} .

better transconductance of the first stage but at the cost of slight degradation of s_{11} , see fig. 9,b.

IV. SUMMARY

A MMIC broadband amplifier based on a 180 GHz f_{\max} P-HEMT technology was designed, fabricated and characterised. The amplifier shows a gain of 11 dB, an input and output reflection coefficient less than -10 dB in a bandwidth of 12 GHz and NF_{\min} less than 4 dB. The simulations of the amplifier noise and s parameters for the set of drain, gate bias points were performed. The best NF_{\min} and s_{21} were obtained for the $V_{D1,2}=1.5\text{ V}$ and $V_G=-0.006$. Simulated s and noise parameters with the wider gate HEMT ($W=4 \times 25\ \mu\text{m}$) at the input yielded an improvement of the NF_{\min} (less than 1.5 dB) at the cost of slight degradation of s_{11} (less than -5 dB over broad band). The grounded gate amplifier based on DO1PH HEMTs with a $W=4 \times 25\ \mu\text{m}$ at the input is a good approach of the broadband low noise amplifier with an adjustable input reflection coefficient.

V. ACKNOWLEDGEMENTS

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VI. REFERENCES

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