

A MOS Model 9 Extension for GHz CMOS RF Circuit Design

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ABSTRACT

This paper presents an extension to the compact MOS model 9 that enables accurate simulation of CMOS RF circuits in the GHz range. The MOS model 9 is generally accepted for low frequency design, but it is quite inaccurate at GHz frequencies if device parasitics are not considered. The presented model is based on a MOS model 9, extended by a network of parasitics, consisting of six resistors, five capacitors, and two JUNCAP diode models. A model developed for a 0.25 μm CMOS technology shows good accuracy in the measured frequency range up to 12 GHz and over a wide bias range. By applying simple rules for scaling of parasitics and a unit transistor layout approach, the model also shows scalability with respect to device width. The model also predicts third-order intercept point with good accuracy, and simulations and measurements on a 2 GHz CMOS amplifier shows also good agreement.

INTRODUCTION

With today's sub-micron CMOS technologies, it is now possible to implement CMOS RFICs for operation in the GHz range [1][2][3]. Although CMOS is notorious for its inferior performance as an RFIC technology, it certainly has very interesting properties for realizing competitive radio transceiver solutions. Among the most important advantages is the possibility of integrating RF analog circuits together with large-scale digital circuits, and also the important potential for low cost. A major obstacle in designing CMOS RFICs is the lack of adequate models that predict device behavior at GHz frequencies. For low frequency analog and digital circuit design, compact MOS models such as MM9 (MOS model 9) [4], BSIM3v3 [5] and EKV [6] are widely accepted, but applying these models at GHz frequencies without parasitic effects gives inaccurate results [7]. A clear example of this is given by the s -parameter plots shown in Fig. 1. This paper describes an extension to the compact MM9 by a network of parasitic elements, which enables accurate prediction of NMOST (n-channel MOS transistor) s -parameters in a wide bias range and for frequencies up to 12 GHz.

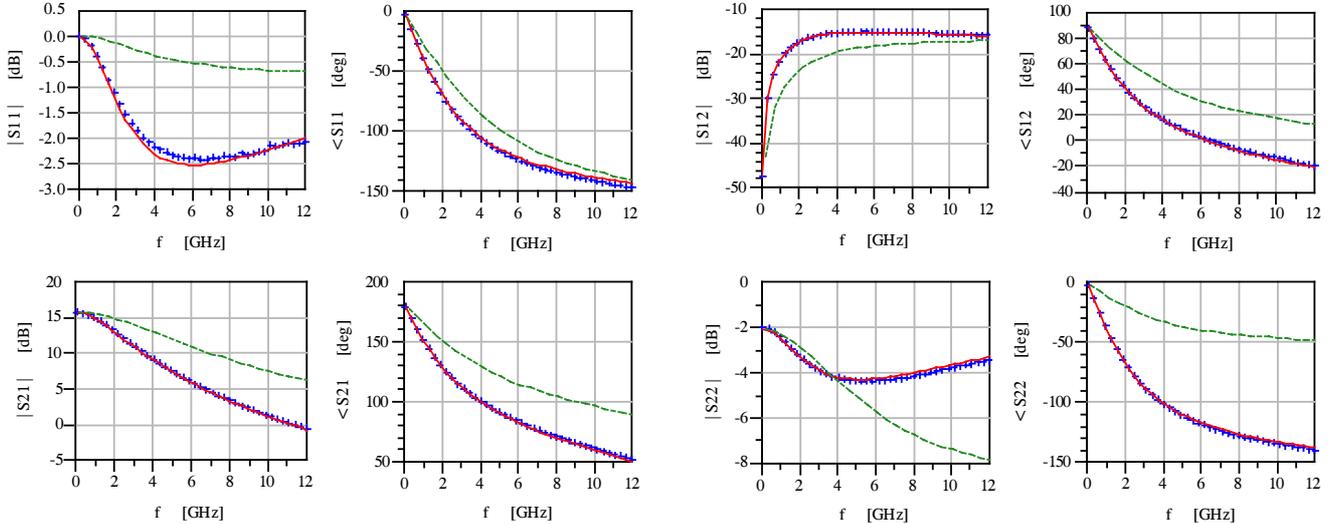


Fig. 1. Simulated and measured s -parameters for a $400 \times 0.25 \mu\text{m}$ NMOST in common-source configuration, biased at $V_{DS}=1.2\text{V}$ and $I_{DS}=8.5\text{mA}$; (+) is measured data, (---) is the standard MOS model 9, and (—) is the new MM9RF model.

THE MM9RF MODEL

The new MM9RF model, shown in Fig. 2, consists of the standard MM9, extended with 5 capacitors, 6 resistors and 2 JUNCAP diode models [4]. Compared with previously published models [7], the addition of the capacitors C_{dse} , C_{dbe} , and C_{sbe} is new. These capacitors accounts mainly for parasitic capacitance due to the interconnect metal in a multi-finger layout, and are important in obtaining adequate accuracy between measured and simulated data.

Based on the model topology in Fig. 2, an NMOST model has been developed for a $0.25 \mu\text{m}$ standard CMOS process. The MM9 and JUNCAP parameters are known a priori, and the parasitic element values have been determined using measured

s-parameters on a $400 \times 0.25 \mu\text{m}$ device. As the MOS transistor is a four terminal device, two port s-parameters have been measured in both CS (common source) and CG (common gate) configurations to enable determination of all the parasitic elements. The measurement configurations are illustrated in Fig. 3. Note that CG enables non-zero back bias ($V_{SB} \neq 0\text{V}$).

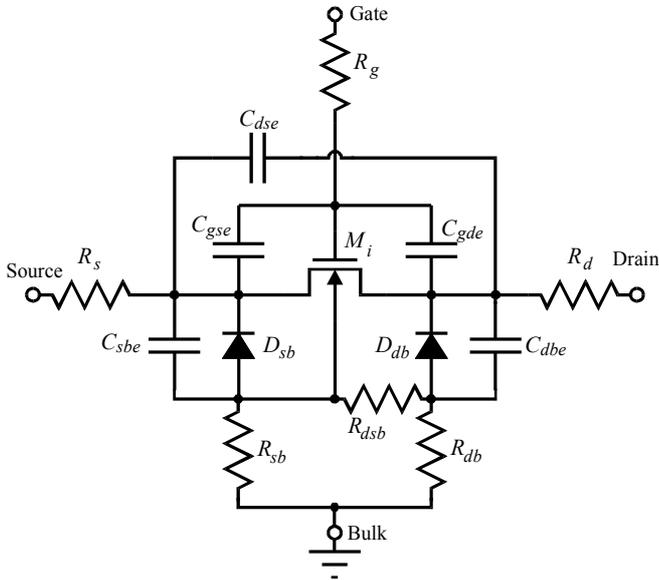


Fig. 2. MM9RF equivalent circuit model, with the MM9 compact MOS model M_i , and the embedding network of parasitics.

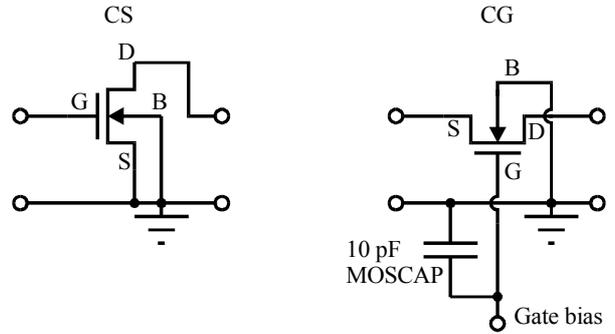


Fig. 3. NMOST in CS and CG measurement configurations.

A set of parasitic element values has been determined, using measured s-parameters in 18 bias points (9 in CS and 9 in CG configuration) spread across the saturated and strong inversion region. The element values were determined by one optimization covering all 18 bias points, using Advanced Design System by Agilent Technologies (Palo Alto, CA). As indicated in Fig. 1 and Fig. 4, excellent agreement has been achieved throughout the measurement range up to 12 GHz, for both CS and CG configurations respectively. Even though the parasitic resistors and capacitors, for simplicity reasons have been assumed bias independent, the model shows good accuracy throughout the saturated and strong inversion region of operation.

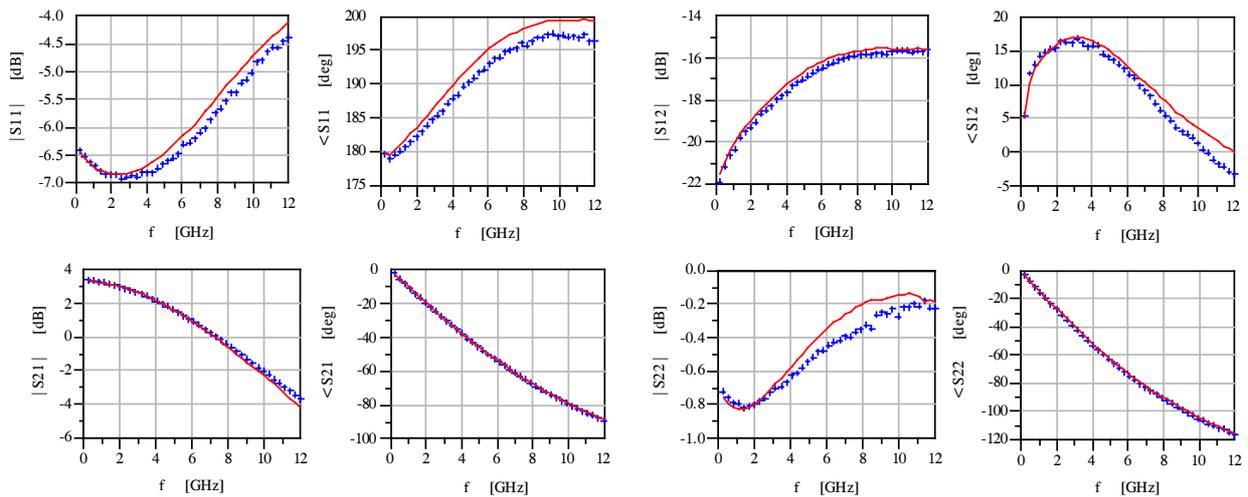


Fig. 4. Simulated and measured s-parameters for a $400 \times 0.25 \mu\text{m}$ NMOST in CG configuration, biased at $V_{DS}=1.8\text{V}$, $V_{SB}=1.0\text{V}$, and $I_{DS}=4.0\text{mA}$; (+) is measured data, and (—) is the new MM9RF model.

An important feature for an NMOST model is that it provides scalability with respect to the device width. To achieve this, a unit transistor layout approach has been used, using a $20 \times 0.25 \mu\text{m}$ unit transistor cell. Larger widths are accomplished by placing a number of this unit transistor in parallel. As reported in reference [8] this technique has proven to give good

scalability of the device parasitics. Assuming a device as an ideal parallel combination of unit transistor cells, the following simple scaling rules may be derived for the parasitic resistances and capacitances for a device of width W :

$$R_{x,W} = R_{x,W_{ref}} \cdot \frac{W_{ref}}{W}; \quad C_{x,W} = C_{x,W_{ref}} \cdot \frac{W}{W_{ref}} \quad (1)$$

where $R_{x,W_{ref}}$ and $C_{x,W_{ref}}$ are the values found for a reference device with width W_{ref} . Using these simple scaling rules for the parasitics, the MM9RF has shown very good scalability with device width. An example of this is shown in Fig. 5, where measured s -parameters for a $200 \times 0.25 \mu\text{m}$ device are compared with simulated data, using the MM9RF model based on the $400 \times 0.25 \mu\text{m}$ device.

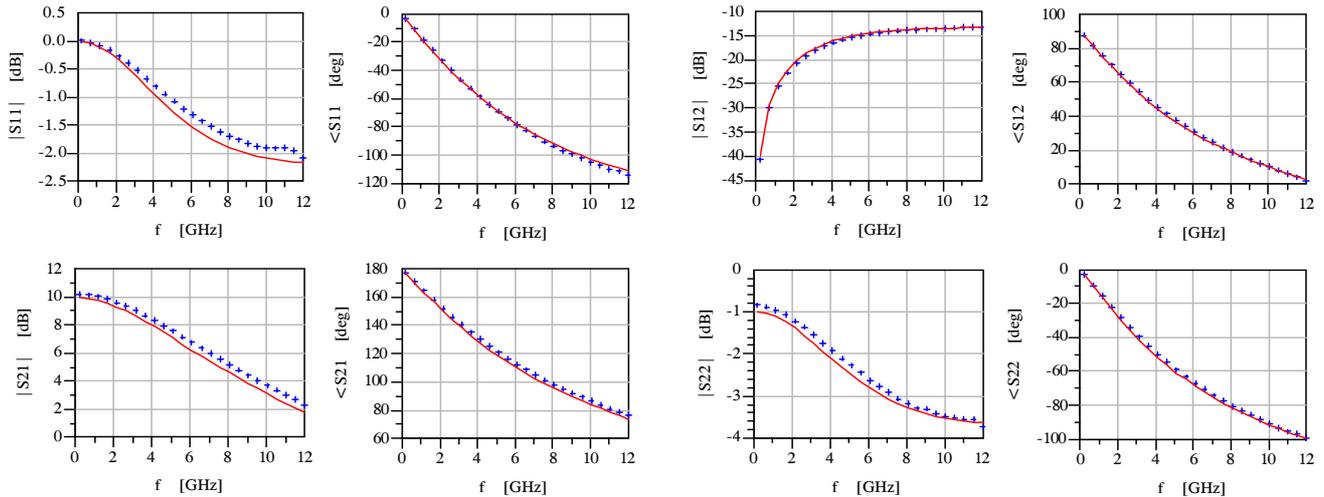


Fig. 5. Simulated and measured s -parameters for a $200 \times 0.25 \mu\text{m}$ NMOST biased at $V_{DS}=2.0\text{V}$ and $I_{DS}=4.0\text{mA}$; (+) is measured data, and (—) is the new MM9RF model with parasitics extracted from measurements on a $400 \times 0.25 \mu\text{m}$ NMOST. The NMOST is in CS configuration.

Another important feature of a NMOST model is its ability to predict non-linear phenomena such as intermodulation. To test the model in this respect, the output 3rd order intercept point was measured for a $400 \times 0.25 \mu\text{m}$ device, in CS and biased at $V_{DS}=1.5\text{V}$, and $I_{DS}=6.1\text{mA}$. The source and load impedances were $50\ \Omega$, and a 2.0 and 2.1 GHz two-tone signal was applied at the input. The 3rd order intermodulation product at 1.9 GHz was measured at the output. Measurements are shown in Fig. 6, and the resulting oIP3 is calculated to be 13.7 dBm. The corresponding simulated value using MM9RF is 15.4 dBm, i.e. only 1.7 dB higher than the measured result, which is a decent accuracy for this parameter.

CIRCUIT EXAMPLE

To evaluate the MM9RF at circuit level, a 2 GHz amplifier was designed and fabricated in a $0.25\ \mu\text{m}$ CMOS process. The amplifier consists of an inductively degenerated cascode input stage and a common source output stage, as shown in Fig. 7. All NMOSTs are modeled using MM9RF, and the passive devices are modeled using equivalent circuit models based on separate on-wafer s -parameter measurements. Measured and simulated data at 2 GHz is listed in Table 1. Shown in Fig. 8, is the measured and simulated power gain $|s_{21}|$, plotted versus frequency.

CONCLUSION

A new extension to a MOS Model 9 compact transistor model has been proposed for accurately predicting MOS transistor behavior up to 12 GHz. The extension consists of 5 capacitors, 6 resistors and 2 juncap diode models. A model for a $0.25\ \mu\text{m}$ CMOS technology has been developed. Using bias independent capacitors and resistors this model achieves good accuracy in a wide bias range. By using a unit transistor layout technique and simple scaling rules for the parasitics, the model also shows very good scalability with device width. The model has also shown fair accuracy in predicting third-order output intercept point. Finally, a circuit level evaluation, using a 2 GHz CMOS amplifier, was conducted and the results show good agreement between measurements and simulations.

ACKNOWLEDGEMENT

The RISC group colleagues at Aalborg University are acknowledged for many helpful discussions. Siemens Mobile Phones and the Danish Academy of Technical Sciences (ATV) are acknowledged for their financial support of this work.

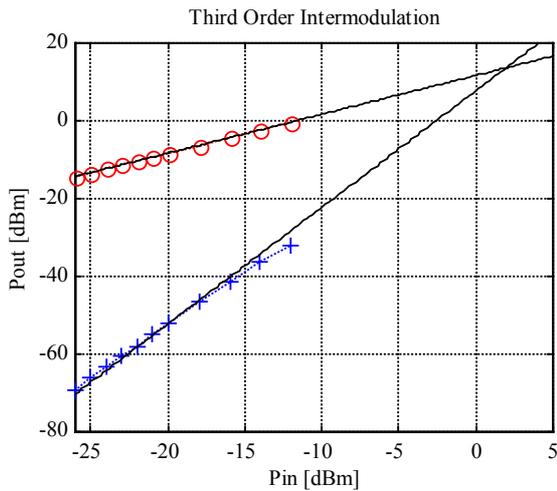


Fig. 6. Measured 3rd order intermodulation on a 400x0.25 μ m NMOST biased at $V_{DS}=1.5$ V and $I_{DS}=6.1$ mA. A two-tone test signal at 2.0 and 2.1 GHz is used (o), and the measured intermodulation product is at 1.9 GHz (+). Extrapolated from measurements, $oIP3$ is found to be 13.7 dBm.

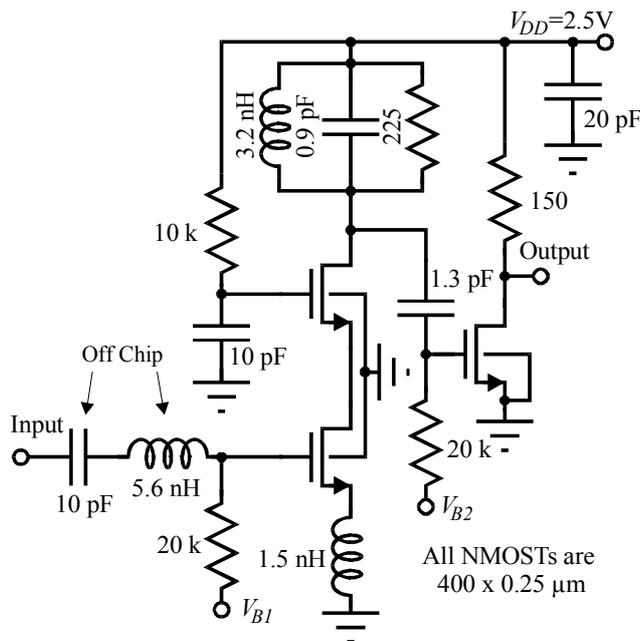


Fig. 7. Schematic of the 2GHz CMOS amplifier. The amplifier is biased at 5 mA in both the input cascode stage and the output common source stage.

$f=2$ GHz	$ s_{21} $ [dB]	$ s_{11} $ [dB]	$ s_{22} $ [dB]	$ s_{12} $ [dB]
Simulated	14.5	-9.4	-12.7	-37.2
Measured	14.7	-7.4	-10.1	-39.7

Table 1. Simulated and measured results at 2 GHz, for the 2 GHz CMOS amplifier.

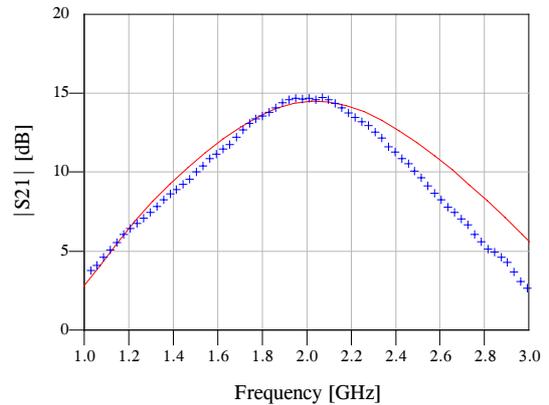


Fig. 8. Measured (+) and simulated (-) power gain, $|s_{21}|$, versus frequency for the 2 GHz CMOS amplifier.

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