High Power Ultra Compact VCO with Active Reactance Concepts at 24 GHz

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***Abstract* — Extremely compact layout and circuit design techniques have been applied to commercially available Si/SiGe hetero bipolar transistor (HBT) MMIC technology. An ultra compact voltage controlled oscillator with a high output power has been realized, addressing the ISM band at 24 GHz. Active reactance concepts have made it possible to realize the layout of this MMIC on an ultra compact area of $300 \times 300\,\mu$m. The voltage control has been provided by a voltage tunable active inductance. To reduce oscillator pushing, a cascode buffer has been added. An output power of +1 dBm at 24 GHz has been achieved.**

I. Introduction

As the cost of analog microwave or millimeter-wave front-end electronics becomes a major factor at increased frequencies of operation, the reduction of the chip area is of prime importance in order to address the low-cost, consumer-oriented market at elevated frequencies. In [1] an integrated ultra compact oscillator design at 16 GHz based on a Clapp oscillator core [2] has been presented, where the typically used on-chip spiral inductance has been replaced by an active inductance.

This work describes a voltage controlled oscillator, which is based on [1]. The voltage control has been realized by a voltage tunable active inductance. The oscillator core is followed by a buffer amplifier stage in order to isolate the VCO core from the load impedance. The chosen active component concept has enabled the realization of the VCO on an ultra compact area of $300 \times 300\,\mu$m.

II. VCO topology

The VCO core, using an active parallel resonance circuit, is followed by a cascode buffer amplifier. A buffer amplifier with a high amplification in the frequency range of 24 GHz to get a high output power level is problematic. To be able to extract high power out of the oscillator core without the need for a high amplification stage, a VCO core with active reactances has been chosen [1].

The used models are a scalable MEXTRAM model for the transistors (see [3], [4] and [5]) and scalable models for the passive elements, describing the electrical behavior of the on-chip transmission lines and capacitances.

A. Active Capacitance

In Figure 1 you can see the detailed circuit schematic of the active capacitance, which represents the core of a Clapp-Gouriet circuit. The transistor T1 is the main transistor, which provides in a certain frequency range a negative resistance at its base terminal. T2 acts as a current source. At the collector terminal of T1, the circuit can be loaded. Negative impedance to the input terminal is generated by capacitive feedback. The input impedance can be approximately described by the equation [6]:

$$Z_{in} \approx \frac{-g_m}{\omega^2 C_1 C_2} + \frac{1}{j\omega\left(\frac{C_1 C_2}{C_1 + C_2}\right)}$$

The base-to-emitter capacitance of transistor T1 has to be taken into account parallel to C_1. Simulation results

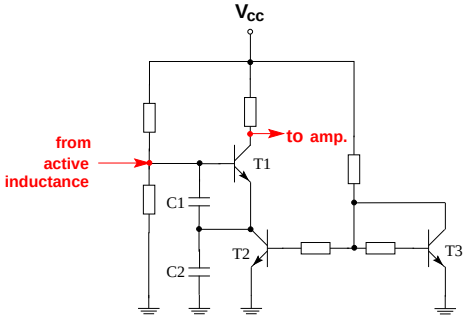

Figure 1: Schematic of the active capacitance

do provide negative resistance to the input terminal from 8 GHz – 17 GHz. The circuit shows at the operation frequency of 24 GHz a positive resistance of about 4 Ω. An inductance with negative resistance is needed for a positive loop gain in the oscillator core.

B. Active inductance

The detailed circuit schematic of the tunable active inductance can be seen in Figure 2. T4 is the main transistor, providing a negative resistance to its emitter terminal. The active inductance is realized as a modified cascode amplifier with a capacitive feedback loaded at the base of the transistor T6 in common emitter configuration. The resulting inductive value of this circuit can be controlled by the potential at the base of transistor T4. Here, the base potential is set by a simple voltage divider referred to the tuning voltage V_{tune}.

The first approach to describe the active inductance is applying the simplest hybrid – π model, neglecting r_e, r_b,

r_c and C_{bc}, and assuming the transistors T4 and T6 have the same size. The impedance to the terminal depicted in Figure 2 is derived as:

$$Z_{ind} \approx \frac{1}{g_m} \cdot \frac{1-\omega^2 C_{be} L}{1-\omega^2 C_{be} L + j\omega L S},$$

where G, C_{be} and L are the transconductance of T4 and T6, base-to-emitter capacitance of T6 and transmission line inductance of the connection of transistor T4 to V_{cc}, respectively. Here, the circuit acts as an inductance for $\omega C_{be} > \frac{1}{\omega L}$. Especially for the active inductance layout parasitics have to be modeled and taken into account accurately. Because of the large signal operation condition, the small signal approach can not describe the whole characteristics of the circuit. A large signal analysis like harmonic balance takes into account the nonlinearities in the transistors, from which the negative resistance of the circuit can be derived to about $-5\,\Omega$.

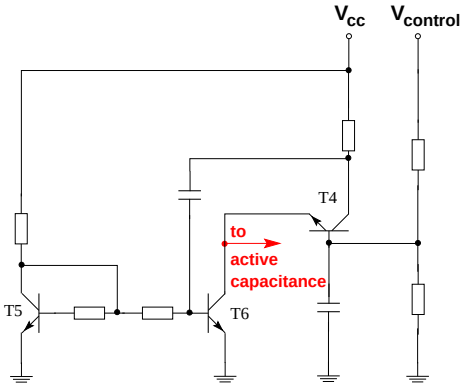

Figure 2: Schematic of the tunable active inductance

C. Cascode topology buffer amplifier

The input impedance of the cascode buffer amplifier shown in Figure 3 is power matched to the output impedance of the active capacitance. The transistor T9 is connected to the supply voltage via an external bias-T. The simulated power gain of the implemented buffer amplifier at 24 GHz is 4.5 dB.

D. VCO Schematic

The circuit diagram of the VCO is completed by connecting the output terminal of the tunable active inductance via an on-chip DC-block capacitance to the input terminal of the active capacitance and loading the active capacitance with the cascode buffer block, which can be seen in Figure 4.

E. Layout

The chip photography of the realized circuit can be seen in Figure 5. The application of active reactances in the VCO design demands accurate knowledge and consideration of parasitic transmission-line-inductances. The layout process itself is an iterative one. Layout parasitics have to be taken into account in the simulation of the circuit shown in Figure 4. The results of the simulation are then used to modify the layout of the circuit again.

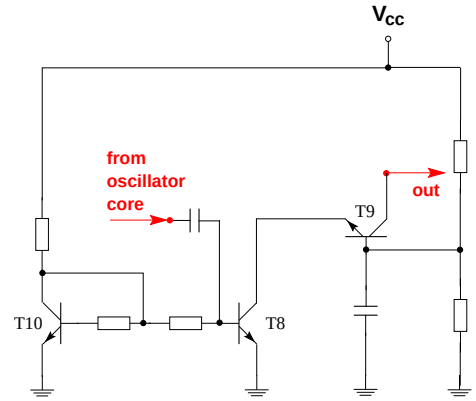

Figure 3: Schematic of the buffer stage in cascode configuration

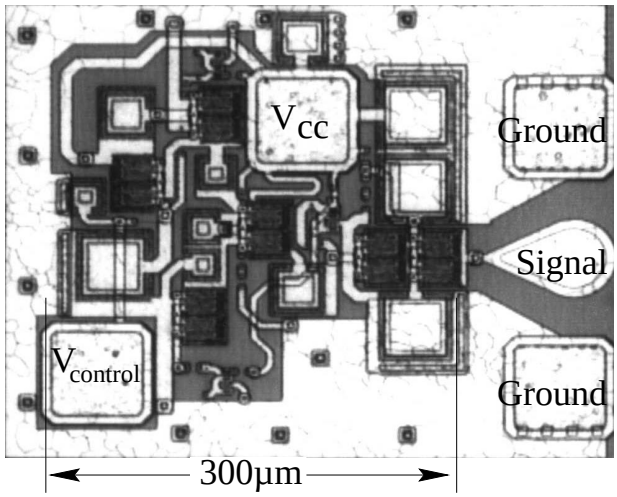

Figure 5: Chip photography of the 24 GHz VCO

F. Results

The VCO has been probed on-wafer, applying the core supply voltage via a needle to the "V_{cc}"-pad and the controll-voltage on the "$V_{control}$"-pad, respectively. The output is connected via a coplanar wafer probe and an external bias-T to the supply voltage. A maximum output power level of $-2.8\,\mathrm{dBm}$ at $24.0\,\mathrm{GHz}$ has been measured. The total attenuation of the measurement setup[1] has been determined to 4 dB. Therefore the actual output power can be estimated to $+1\,\mathrm{dBm}$. An overall current consumption of 55 mA at a supply voltage of 3.6 V has been determined. The spectral output power can be seen in Figure 6. The phase noise is $-99\,\mathrm{dBc/Hz}$ at $10\,\mathrm{MHz}$ offset from the carrier, measured on wafer. However it is

[1] ground-signal-ground probe, bias-T, coaxial cable and two interconnects

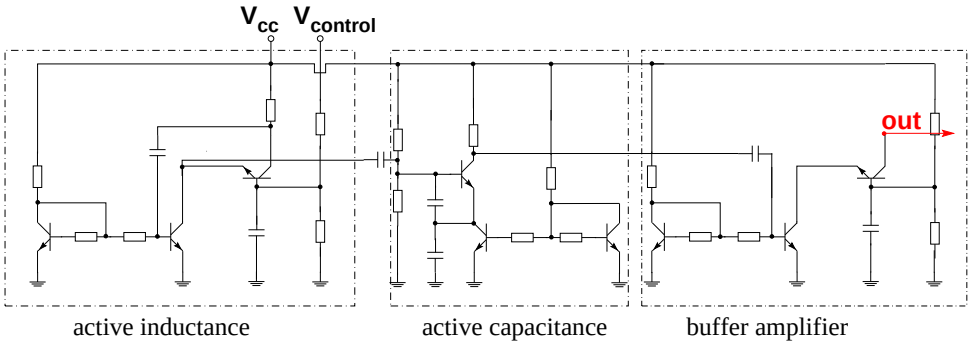

Figure 4: Schematic of the complete VCO

believed to be dominated by low-frequency pick-up in the probe needles.

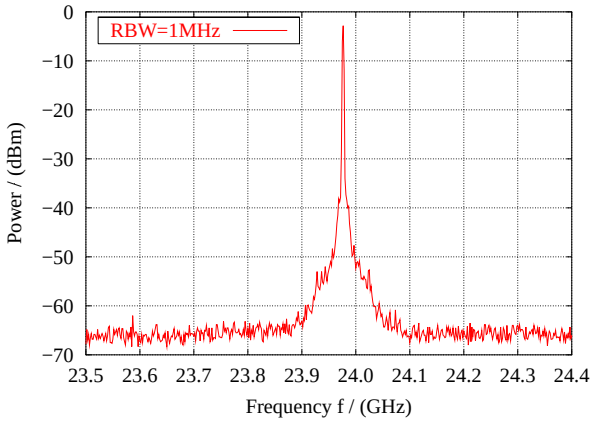

Figure 6: Spectral output of the VCO with an output power of $-2.8\,\mathrm{dBm}$ at $24.0\,\mathrm{GHz}$ (not corrected for measurement losses)

The results of the frequency respons can be seen in Figure 7. The control voltage is above the supply voltage because of the way of biasing the transistor T4 in Figure 2 by a voltage divider. At $V_{control} = 4.2\,V$ the transistor T4 and at $V_{control} = 6.0\,V$ the transistor T6 of the active inductance is in a soft-breakdown condition, respectively.

III. Conclusion

Using a mature commercially available Si/SiGe HBT process, an oscillator concept based on the Clapp-Gouriet circuit with a buffer amplifier has been realized. The inductance in the resonant circuit has been realized as a tunable active inductance. The chip area of the VCO was only $300 \times 300\,\mu m^2$. This reduction in chip area has been enabled by the replacement of the spiral inductor by an active inductance. Therefore high output power can be extracted out of the oscillator core. An output power level of $+1\,\mathrm{dBm}$ at $24\,\mathrm{GHz}$ has been determined, addressing the ISM-Band. In the future, work will concentrate on more careful phase noise characterization and optimization.

We envision the use of this robust and compact VCO design in extremely compact and cheap SiGe MMICs, e.g.

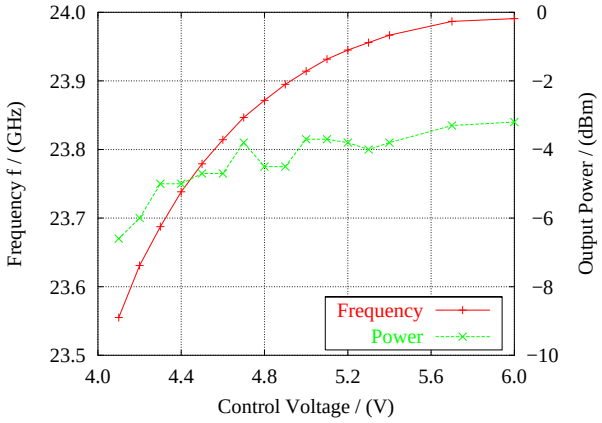

Figure 7: Frequency response of the $24\,\mathrm{GHz}$ VCO (not corrected for measurement losses)

for RFID, simple radar or close-range transponder applications.

IV. References

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