A Miniaturized 0.5-Watt Q-band 0.25-µm GaAs PHEMT High Power Amplifier MMIC

A. Bessemoulin, Member, *IEEE*, P. Quentin, H. Thomas, and D. Geiger

United Monolithic Semiconductors, route départementale 128 – BP46,
F-91401 Orsay Cedex, France
Ph. (+33) 1 69 33 05 46 – Fax. (+33) 1 69 33 05 52
email: alexandre.bessemoulin@ums-gaas.com

The performance of a very compact power amplifier MMIC for Q-band applications is reported. Using a 4-inch 0.25-µm GaAs power PHEMT process, this 4-stage amplifier achieved a linear gain of 19 dB over the 36 to 45 GHz frequency range, with an output power at 1-dB gain compression of 26 dBm (P_{-1dB}=400 mW), and a saturated output power of 0.5 Watt (P_{sat}=27 dBm), for a chip size of only 2.25 mm^2 (1.25 × 1.8 mm^2). Compared to state-of-the-art power amplifier MMICs operating in the 36-43 GHz frequency range, the combined output power- and gain- densities per chip area are nearly a factor two higher, namely 220 mW/mm^2 and 8.5 dB/mm^2.

INTRODUCTION

LMDS and MVDS markets have created a demand for cost effective power amplifier MMICs at Ka- and Q-band frequencies (e.g. [1]). Considering size as the main driving cost of a MMIC, the compact power amplifier MMIC presented in this paper has been designed to address this requirement in the upper LMDS band (38.5-43.5 GHz), using the UMS 0.25-µm gate length GaAs power PHEMT production process. Indeed, whereas at these frequencies, 0.15-µm PHEMTs are usually preferred [2-4], quarter-micron gates using optical lithography are much easier and faster to process than direct E-beam write ones, and therefore less expensive. Nevertheless, the key technology issues in combining simultaneously a small chip size and high power, were the use of:

- thin 70-µm GaAs substrate for smaller transmission line elements, and reduced coupling in comparison to 100-µm substrate thickness technologies,
- small via-holes, and short distance between vias, allowing the placement of microstrip elements with minimum spacing,
- novel compact PHEMT devices with individual source vias (ISV), for high gain, and very good thermal properties.

Furthermore, the high integration density was achieved not only thanks to appropriate matching networks that incorporate lumped elements, but also with compact topologies optimized with the support of 2D- and 3D electromagnetic (EM) simulations [5].

PROCESS TECHNOLOGY

The MMIC fabrication is based on our selective double-recess / double-side-doped channel power PHEMT process, using 0.25-µm Aluminum T-gates on 4'' wafers (PPH25). The main electrical characteristics of this process are summarized in Table I.

Table I. Electrical parameters of UMS 0.25-µm Power PHEMT process.

DC Parameters	Typical values
Peak G_m	450 mS/mm
V_{gs} @ Peak G_m	-0.1 V
I_{ds} @ Peak Gm	240 mA/mm
I_{dss}	270 mA/mm
$I_{ds,max}$	520 mA/mm
BVGD @ 1 mA/mm	14 V

The MMICs are realized on 70-µm substrate, with two thick gold metallization levels, 30 Ω/□ TaN thin film resistors, 250 pF/mm^2 Silicon Nitride MIM capacitors, airbridges, and 20-µm via-holes. A compact 0.3-mm gate-width transistor, with vias under every source, is used as unit cell. Due to the multiple thermal shunts and grounding ensured with the vias, such a device results in lower junction temperature, and a negligible source inductance (below 5 pH), leading to higher gain and reliability. The benefit of this compact ISV PHEMT is illustrated in Fig. 1: biased at peak transconductance, under 4-, 5-, and 6-V drain voltage, a maximum available gain (MSG/MAG) of respectively 9.5-, 8.3-, and 7.3 dB is achieved at 45 GHz, with an extrinsic maximum frequency in excess of 65 GHz, which is very attractive for a 0.25-µm GaAs PHEMT double recess process.

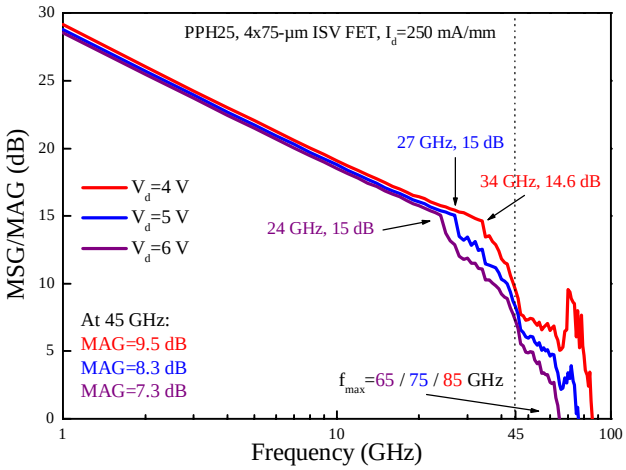

Fig. 1: Measured MSG/MAG of a 4 x 75 µm ISV PHEMT device at peak transconductance, and I_d=250 mA/mm.

CIRCUIT DESIGN

The Q-band MMIC PA (Fig. 2) consists of four 4×75-µm devices, driven by three successive stages having a gate width ratio of 2:1, for a total gate periphery of 2.4 mm, and a chip size of only 2.25 mm^2 (1.25×1.8 mm^2). Prior to circuit optimization, special considerations were made on choosing compact matching topologies that occupy as much the remaining GaAs area as possible. Critical parts such as very close instances and short transmission lines were simulated with 2D EM software.

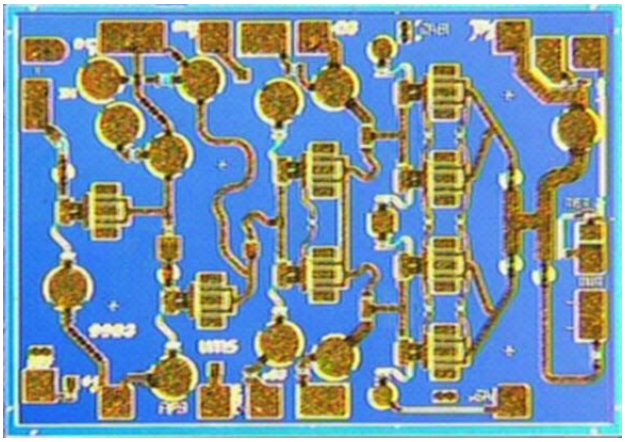

Fig. 2: Chip photograph of the 0.5-Watt 36-45 GHz Power Amplifier MMIC (chip size is 1.8×1.25 mm^2 = 2.25 mm^2).

Based on the optimum power transfer and load line approaches, rigorous design and layout methods were considered in the optimization of power, gain and bandwidth. While the output stages were designed to deliver the maximum output power, the first and second stages were optimized for gain flatness. For flexible impedance matching and size reduction, the matching networks were realized using capacitively loaded transmission lines [1,2]. However, accurate models for MIM shunt capacitors over vias are essential at this frequency range. Scalable models were firstly derived from 3D EM simulations using Microwave Studio®, and verified with the broadband characterization of test structures. The MIM shunt capacitor model is a simple T-network with two series inductors, and a parallel capacitor in series with an inductor. The figure 3 shows the comparison between the measured and modeled S-parameters of a MIM shunt capacitor, having a nominal capacitance of 200 fF. As illustrated, a very good agreement is achieved up to 60 GHz, with an absolute magnitude/phase error below 0.5 dB ∠ 5°.

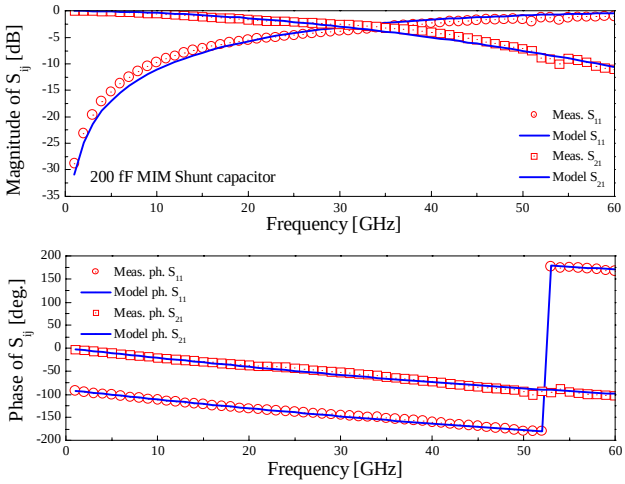

Fig. 3: Comparison between measured and modelled S-parameters of a 200-fF MIM shunt capacitor, over the 0.5-60 GHz frequency range.

Stability was also a primary concern; K-factor, and the Nyquist determinant factor analysis (NDF, [6]), in combination with large on-chip bypassing capacitors and resistive loading, were used to prevent low frequency-, parametric-, and odd-mode oscillations, resulting in the unconditional stability of the amplifier above the PHEMT device f_{max}. Additionally, for output power monitoring, a compact detector was integrated on the chip.

MEASURED PERFORMANCE

The MMIC amplifiers were tested on-wafer continuous wave (CW) for small signal S-parameters, and with pulsed DC drain for power. The Fig. 4 shows the small signal gain, input- and output return losses of the amplifier. The measurements were performed under low bias conditions, namely V_d=2.0 V and I_d=400 mA, in order to avoid thermal problems. From 36 to 45 GHz, the gain is greater than 21 dB with relative good on-wafer input-, and output matching; it is worth mentioning that I/O matching networks were directly optimized for the

compensation of bond wire interconnects, as finally used in mounted devices.

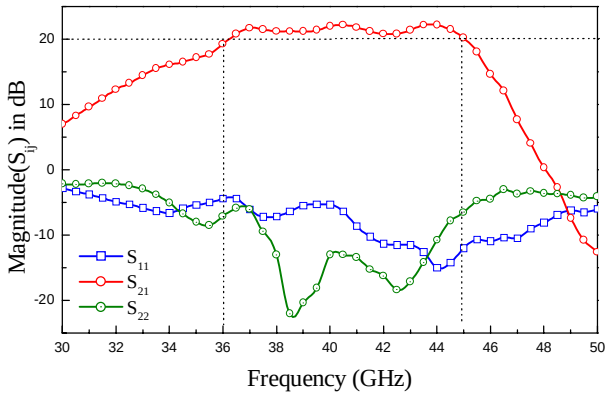

Fig. 4: On-wafer measured small signal gain, input- and output return losses versus frequency of the 35-45 GHz power amplifier at V_d=2.0 V, I_d=0.4 A.

Fig. 5 and 6 show the measured gain, and output power under pulsed DC drain (pulsed width = 20 µs, duty cycle = 25 %), for two wafers coming from two different lots. At 41 GHz (i.e. middle of the bandwidth), P_{in}=+8 dBm, V_d=5.8 V, and for a total supply current of 570 mA, the output power averages 26.5 dBm, with an associated gain of 18.5 dBm. At the same time, the output power detector produces a voltage ranging from 10 mV to 500 mV, which corresponds to an output power increasing from 10 to 27 dBm. As illustrated also from Fig. 5 and 6, for more than 550 and 600 cells distributed uniformly across two 4'' wafers, excellent uniformity and RF functional yield above 75 % taking P_{out} > 26 dBm as screening criteria, are achieved.

Finally, Fig. 7 shows the measured S-parameters of the power amplifier MMIC, mounted in a 40-GHz JIG test fixture, at V_d=5 V and I_d=650 mA. As shown, the small signal insertion gain of the whole test fixture (including losses) averages 18 dB from 37.5 to 45 GHz.

CONCLUSION

A compact 4-stage 36-45 GHz 0.25-µm GaAs PHEMT power amplifier MMIC with 500-mW output power has been presented. With a chip size of only 2.25 mm^2, power- and gain- densities nearly twice superior to the best previously reported results (145 mW/mm^2 and 4.3 dB/mm^2 in [1]), it establishes the state-of-the-art for PA size reduction, and a new benchmark for cost-effective power MMICs at Q-band, as illustrated in Table II.

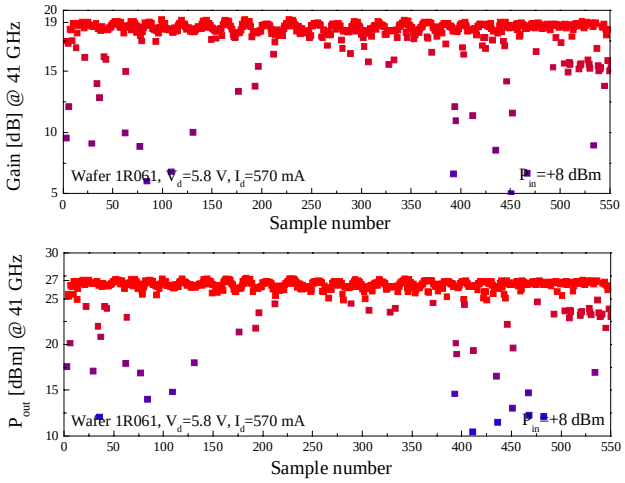

Fig. 5: On-wafer gain and output power mapping of wafer n°1 (554 cells) at 41 GHz, P_{in}=+8 dBm, V_d=5.8 V, and I_d=570 mA.

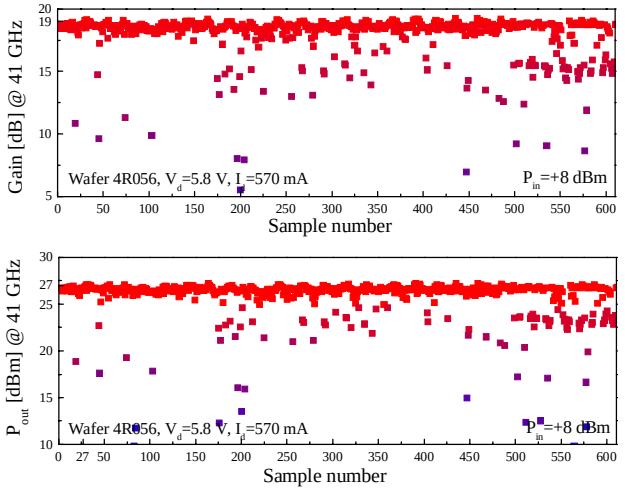

Fig. 6: On-wafer gain and output power mapping of wafer n°2 (608 cells) at 41 GHz, P_{in}=+8 dBm, V_d=5.8 V, and I_d=570 mA.

Table II. Comparison of microstrip 0.5~1.0-Watt Q-band power amplifier MMICs at 40 GHz.

P_{-1dB} (dBm)	Gain (dB)	Chip size (mm^2)	P_{-1dB} (mW/mm^2)	Ref.
26	15	3.48	145	[1]
25.5	11	4.28	81	[2]
28	24	12.4	36	[3]
27	13	4.3	116	[4]
26	18	2.25	220	**This work**

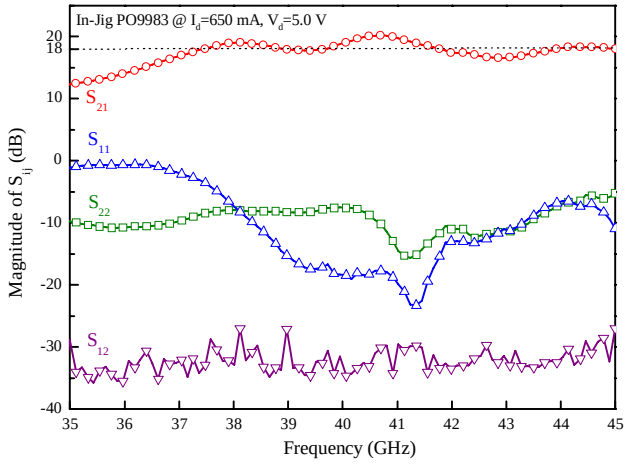

Fig. 7: Measured S-parameters of the JIG test fixtured PA at V_d=5 V, and I_d=650 mA, over the 35-45 GHz frequency range.

REFERENCES

(1) C.F. Campbell, S.A. Brown, "A Compact, 40 GHz 0.5 W Power Amplifier MMIC," in *21st 1999 IEEE GaAs IC Symp. Dig*, pp. 141-143.

(2) A. Bessemoulin et al., "1-Watt Ka-Band Coplanar High Power MMIC Amplifiers using 0.15 µm GaAs PHEMTs," in *22nd 2000 IEEE GaAs IC Symp. Dig*, pp. 227-230.

(3) Raytheon, RMP39000 product datasheet, Dec. 2001.

(4) Velocium, APH474 product datasheet, Jan. 2002.

(5) A. Bessemoulin et al., "1-Watt Broad Ka-band Ultra Small High Power Amplifier MMICs Using 0.25 µm GaAs PHEMTs," to be published in *24th 2002 IEEE GaAs IC Symp. Dig.*, October 20-23, 2002. Monterey, CA, USA.

(6) A. Platzker, W. Struble, "A Rigorous Yet Simple Method for Determining Stability of Linear N-port Networks," in *15th 1993 IEEE GaAs IC Symp. Dig*, pp. 251-254.

ACKNOWLEDGEMENT

The authors would like to acknowledge the contribution of their colleagues from the technology department, for professional MMIC processing, S.R. Nelson, Nanowave Inc., Richardson/USA, and C. Schwoerer, now with the Fraunhofer-IAF, Freiburg/Germany, for fruitful discussions, and the President & CEO of UMS, Prof. H. Daembkes for his continuous encouragement of this work. D. Geiger is now with the Gesellschaft für Diamantprodukte – Daimler Chrysler Research Center, Ulm/Germany.