

# Vertical Silicon K-Band CPW Through-Wafer Interconnects

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*With the increase in production volume of RF devices (e.g. for automotive applications), packaging and interconnection become more and more important. Furthermore, new system concepts such as chip-on-chip or RF-MEMS demand new packaging strategies. This paper presents a vertical silicon micromachined RF CPW through-wafer feedthrough with excellent performance in the K-band. In particular, the feedthrough demonstrates an insertion loss of 0.16dB and a return loss of 20dB at 25GHz. A lumped element model was developed and was evaluated with measurements.*

## INTRODUCTION

In standard IC industry the packaging issue is a well known and highly investigated topic. Due to a great number of pieces, several types of interconnection are standardized with regard to electrical performance, materials, reliability, and dimensions. For RF devices the standardized frequency range reaches up to some GHz (e.g. 2GHz for mobile communication) [1]. For higher frequencies, proven concepts such as the flip-chip technology are available, but no standards are defined [2]. This is due to the problems that occur when the wavelength approaches the dimensions of the interconnection 'wires'. The electrical performance decreases and a large increase can be seen in transmission and return losses. Therefore, the design of RF packaging requires special considerations for the electromagnetic waves.

RFICs with passivated surface can be connected to the circuitry via flip-chip integration. Problems emerge with the connection of innovative systems like chip-on-chip (Fig. 1) or RF-MEMS [3], that have a topography on the top surface or require hermetic packaging.

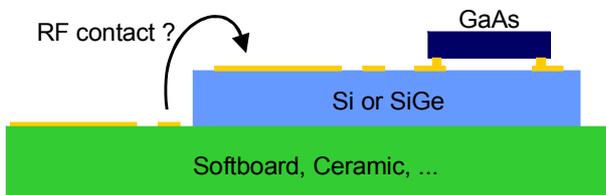


Fig. 1. Principle structure of a chip-on-chip system.

Ceramic packages with good performance have been demonstrated, but the resulting costs are not acceptable for mass production [4]. Another presented possibility is to use through-wafer CPWs with KOH-etched vias [5]. To overcome the limited bandwidth of wire bonding, the costs of ceramic packages, and the large size of KOH

vias, a concept of a vertical silicon CPW through-wafer via is presented for the K-Band.

## DESIGN OF THE CPW VIA

For the interconnection of the lower and upper CPWs we chose a CPW via. Thus, the first attempt was to continue the CPW through the silicon wafer (see Fig. 2).



Fig. 2. Sectioned illustration of a CPW via.

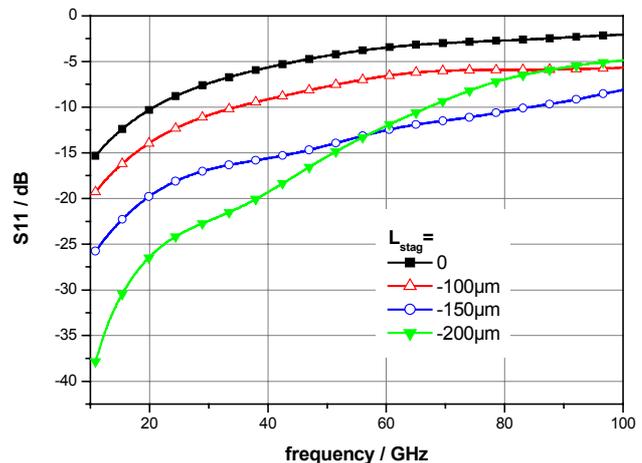


Fig. 3. Calculated return losses of a single CPW via under variation of the staggering length.

The quality of a RF interconnection can be judged by high transmission performance and low reflection of the RF signal. Examining these parameters, numerical simulation of this first structure with MAFIA (CST) showed unsatisfactory performance in the >20GHz region (Fig.3, filled squares).

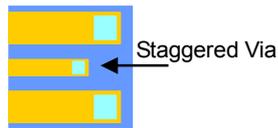


Fig. 4. Top view of the CPW with a staggered via.

To optimize the structure we applied a design method known from RF flip-chip technique as ‘staggered bumps’ [2], which moves the signal bump out of plane relative to the mass bumps for minimizing the reflected power at the flip-chip transition. Applied to the RF via, we moved the signal via (so to speak ‘staggered via’ Fig.4).

Fig.3 shows the results of the simulations. For a length of 150 $\mu$ m an optimal result over a wide frequency range can be obtained.

### FABRICATION PROCESS

The fabrication process involves the combination of bulk micromachining and deposition of metal layers. A 200 $\mu$ m thick high-resistivity double-side polished silicon wafer is used as substrate. The upper side is coated with 30/900nm of TiW/Au and the CPWs are electroplated (3 $\mu$ m Au) in photoresist trenches. The vias are trenched with an RIE plasma etcher (Bosch process) with etch stop at the metalization of the upper side (Fig.5).

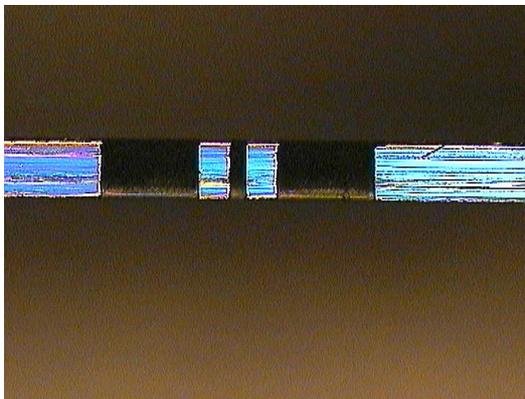


Fig. 5. Cut view of a trenched CPW via.

30/900nm of TiW/Au is deposited at the lower side and in the vias. 3 $\mu$ m Au electroplating builds the lower CPW and the via metalization.

Self-evidently, DC contacts of nearly any shape can be manufactured with the same process steps.

### MEASURED RESULTS

In order to ensure contacting possibilities with the measurement probes the processed test fixture is designed as a double via. Fig.6 shows a schematic of this structure.

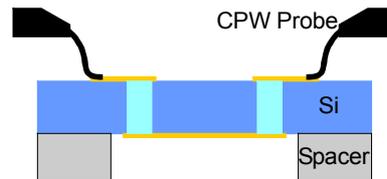


Fig. 6. Schematic of the double via layout and the measurement arrangement.

During measurement, glass spacers of 1mm thickness are applied under the wafer to prevent the lower CPW from short-circuiting and to minimize the detuning influence of the metal chuck. For the measurements, a HP 8510C vector network analyzer is utilized with 150 $\mu$ m pitch Cascade coplanar GSG probes. LRM calibration is performed using a Cascade calibration substrate.

Fig.7 shows the measurement data of the staggered vias. As can be seen, a staggering length of 150 $\mu$ m improves the transmission as it was calculated by the simulation.

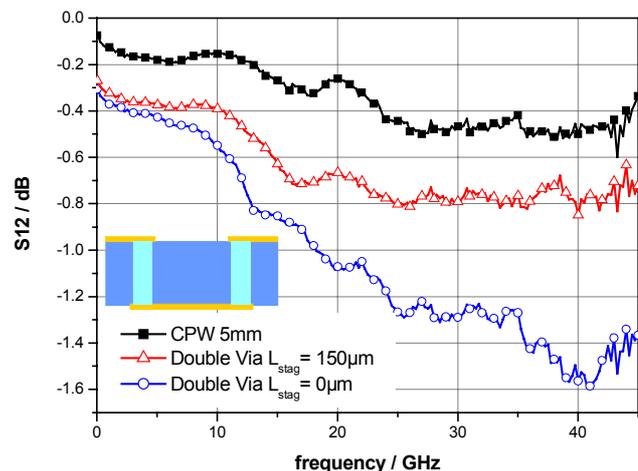


Fig. 7. Measured insertion loss of a CPW (5mm), a double via structure without staggered bumps, and with a staggering length of 150 $\mu$ m.

Deembedding the double via losses with the losses of a corresponding CPW, an insertion loss per via of 0.16dB at 25GHz is achieved.

### MODELING

For better physical insights and for further optimization it is very helpful to generate an electrical model of the CPW via. The model shown in Fig.8 consists of an ideal transmission line at each the beginning, the middle part, and the end. The vias are modeled with lumped elements consisting of a series inductance, a series resistance and two parallel capacitances.

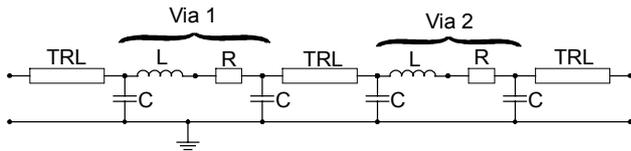


Fig. 8. Lumped element model of the double via structure (TRL: transmission line).

A comparison between the measurement and the model can be seen in Fig.9 (return loss) and Fig.10 (insertion loss). As discernible, the model works well. Measurement data was taken from a CPW with 100 $\mu$ m signal line width and a staggering length of 150 $\mu$ m. The corresponding set of parameters is given in Table I. Compared to earlier published values of flip-chip bumps calculated by a FDTD simulation [6], they are of the same order.

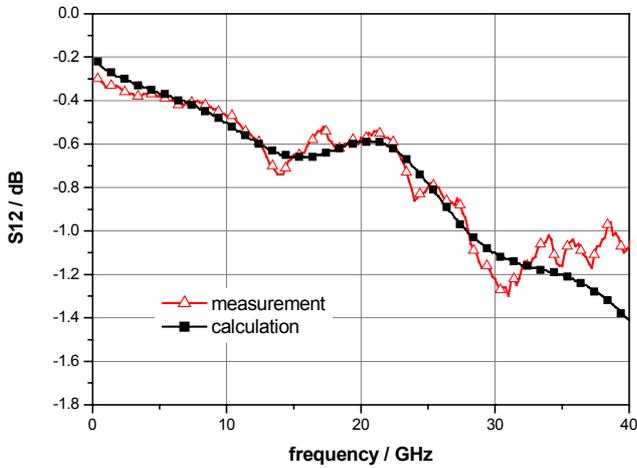


Fig. 9. Comparison of the return loss between measurement and lumped element model.

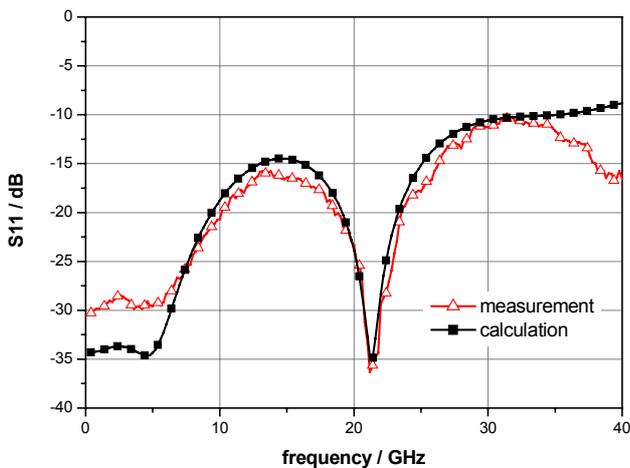


Fig. 10. Comparison of the insertion loss between measurement and lumped element model.

A similar double via structure with identical transitions was designed to verify the model. Here, the lower CPW is shorter, compensated by longer upper CPWs. Compared to the same set of parameters except for the length of the CPWs, the model fits well too.

Table I  
Model Parameters

| Vias                              |            |         |
|-----------------------------------|------------|---------|
| L                                 | R          | C       |
| 120 pH                            | 1 $\Omega$ | 7 fF    |
| Left and right transmission lines |            |         |
| Z                                 | $\alpha$   | length  |
| 46 $\Omega$                       | 16 dB/m    | 1.85 mm |
| Middle transmission line          |            |         |
| Z                                 | $\alpha$   | length  |
| 50 $\Omega$                       | 16 dB/m    | 1.5 mm  |

### Tuning the frequency range

The measurements show low return losses in a limited bandwidth. With a little modification in the model (adding series capacitances into the via model), the frequency range can be tuned to higher frequencies.

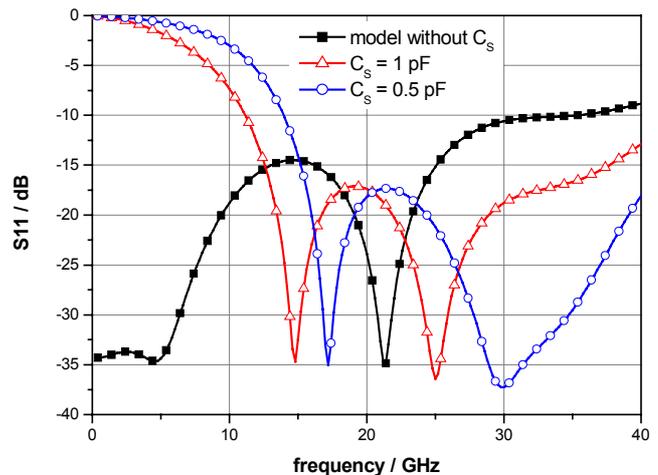


Fig. 11. Tuning the frequency range with series capacitances.

In Fig.11 calculated return losses are shown with series capacitances of 0.5pF and 1pF. In this way, the frequency range can be tuned up to 40 GHz.

But how to integrate these capacitances into the transition?

For example, they could be formed by a dielectric between the via metalization and the upper CPW (Fig.12). E.g. with silicon dioxide as dielectric ( $\epsilon_r \approx 3.8$ ) a 50x50 $\mu$ m via would require a thickness of approximately 180nm to build a 0.5pF capacitance. The required values are feasible for standard semiconductor processes.

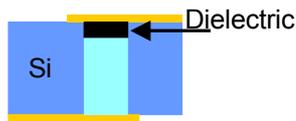


Fig. 12. Concept for via-integrated series capacitance.

## CONCLUSION

A vertical feedthrough for RF signals on silicon wafers was presented. The fabrication process has been developed enabling measured transmission losses of a double via with a CPW length of 5mm of 0.7 dB at 25GHz. Deembedding the CPW losses, a single transition performs with an insertion loss of 0.16dB. A lumped element model which is in good agreement with the measurement was developed and verified. Using this model, we were able to elaborate a frequency tuning concept that can be manufactured by standard semiconductor processes.

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