POWER BALANCE IN HIGH EFFICIENCY PAs

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ABSTRACT

Power balance considerations will be discussed, stressing the relevance of the power dissipated at harmonic frequencies. The high frequency operation of two different strategies for high efficiency PA design will be considered, Class E and Class FG respectively, and their performances compared by means of design examples performed on a single-stage power amplifier operating @ 5 GHz.

I. INTRODUCTION

The power amplifier (PA) is a crucial element of transmitter units; its main design requirements being a high power efficiency to reduce operating costs, to improve battery lifetime and to ease thermal management, coupled with a high power gain and power output levels to reduce the number of amplifier stages and unit size and weight. Such requirements are often contrasting ones, therefore demanding a design compromise on achievable performances. A suggested solution to improve both efficiency and output power resides in the use of harmonic tuning strategies, consisting in the design of optimised matching networks, both at the input and output ports, accounting for the fundamental load impedances and harmonic terminations [1]. This approach, although theoretically investigated in ideal cases [2], is not completely clarified in its practical use for high frequency applications, i.e. when the operating frequency increase: in this case the number of the harmonic terminations that can be effectively controlled is limited by practical considerations. Moreover, basic constraints imposed on the high efficiency goal have to be applied. In this paper such constraints will be focused starting from power balance considerations, and analytic results [3] previously obtained will be exploited.

II. POWER BALANCE CONSIDERATIONS

Harmonic tuning strategies assume the active device acting as a voltage controlled current source; load networks are usually designed following different criteria: conjugate matching condition apply between the external source and the device for the input network; the output network is designed to minimise the dissipated power in the active device, therefore increasing the power delivered to the load at fundamental frequency (e.g. Class F strategy [4]). This approach is not completely exact, as it will be shown in the following, since minimisation of the dissipated power does not suffice.

A schematic PA configuration is depicted in Fig.1. In this scheme, the device is driven by an external *rf* source, delivering the input power (P_{in}), and converts *dc* power (P_{dc}) into *rf* output power at fundamental frequency ($P_{out,f}$). Such power conversion is accounted for by the drain (η) and power added (η_{add}) efficiencies. For simplicity, the analysis will be carried out considering the maximisation of the drain efficiency η, since the power added efficiency η_{add} requires the relationship between $P_{out,f}$ and P_{in}, thus implying a complication in the equations.

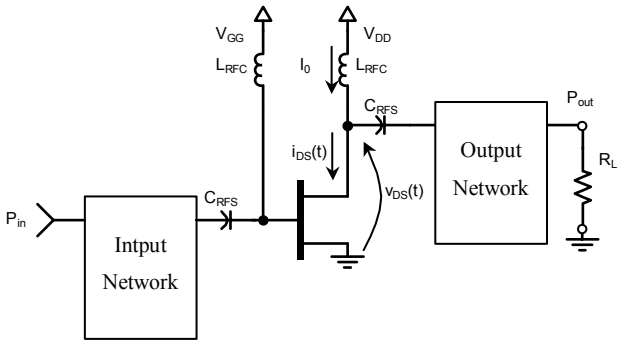

Fig.1: Simplified PA scheme

Assuming an operating frequency *f* in periodic regime, drain current and voltage waveforms are expressed as :

$$i_{DS}(t) = I_0 + \sum_{n=1}^{\infty} I_n \cdot \cos(n\omega t + \psi_n) \qquad (1a)$$

$$v_{DS}(t) = V_0 - \sum_{n=1}^{\infty} V_n \cdot \cos(n\omega t + \varphi_n) \qquad (1b)$$

where $\omega=2\pi f$, ψ_n and φ_n are the phases of the current (I_n) and voltage (V_n) n-th harmonic components linked through the output loads Z_n :

$$\mathbf{Z_n} = Z_n \cdot e^{j\phi_n} = \frac{V_n \cdot e^{j\varphi_n}}{I_n \cdot e^{j\psi_n}} = \frac{V_n}{I_n} \cdot e^{j(\varphi_n - \psi_n)} \qquad (2)$$

and

$$I_0 = \frac{1}{T}\int_0^T i_{DS}(t)dt \qquad V_0 = \frac{1}{T}\int_0^T v_{DS}(t)dt = V_{DD} \quad (3)$$

From the previous expressions, the supplied *dc* power and dissipated power on the active device are:

$$P_{dc} = V_{DD}\cdot I_0 \qquad P_{diss} = \frac{1}{T}\int_0^T v_{DS}(t)\cdot i_{DS}(t)\,dt = P_{dc} - P_{out,f} - \sum_{n=2}^{\infty} P_{out,nf} \quad (4)$$

where

$$P_{out,nf} = \frac{1}{2}V_n I_n \cos(\varphi_n - \psi_n) \quad n = 1,2,... \quad (5)$$

represent the active power delivered from the device to the output matching network at fundamental ($P_{out,f}$) and harmonics ($P_{out,nf}$), thus spreading in frequency. Drain efficiency η can be therefore expressed as:

$$\eta = \frac{P_{out,f}}{P_{dc}} = \frac{P_{out,f}}{P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf}} \quad (6)$$

From the expression above, maximum drain efficiency (η=100%) can be obtained *if and only if* the following conditions are *simultaneously* fulfilled:

$$P_{diss} = \frac{1}{T}\int_0^T v_{DS}(t)\cdot i_{DS}(t)dt = 0 \quad (7a)$$

$$\sum_{n=2}^{\infty} P_{out,nf} = \frac{1}{2}\sum_{n=2}^{\infty} V_n I_n \cos(\varphi_n - \psi_n) = 0 \quad (7b)$$

Importance of condition (7b) is clear if square waveforms are assumed for both output current and voltage (i.e. the output network is simply resistive at any frequency). In this case, while P_{diss}=0 (no waveforms overlapping), maximum drain efficiency is 81.1% only, due to power dissipation on output network at harmonic frequencies ($P_{out,mf}$≠0 for m odd).

As a conclusion, the condition P_{diss}=0 does not suffice to assure maximum theoretical drain efficiency, as often assumed in the past. It is also necessary that the output power dissipated at harmonic frequencies is zero. Thus, the condition to obtain maximum drain efficiency can be formulated in the following equivalent ways: maximise fundamental output power $P_{out,f}$ or minimise the *sum* of P_{diss} and $P_{out,nf}$ (n>1).

III. Sample Harmonic Tuning Approaches

In the ideal Class F [2] approach, both the conditions (7) are fulfilled, since waveforms overlap is avoided (P_{diss}=0) and V_nI_n=0 for n>1, thus obtaining η=100%. Similar result is theoretically obtained swapping voltage and current, as in the "inverse Class F" amplifier [5]. This is only an idealised approach. In fact, if a more realistic one is adopted, in which the voltage and current harmonic components are related through physically realizable output harmonic load impedances, it can be demonstrated that, using a Class C bias, a Class F approach is practically detrimental for the efficiency and that in real device, also a bias condition near Class B could not be useful [6].

In Class E approaches, the active device is operated as a switch (cfr. [7] for typical waveforms). Condition (7a) is satisfied since there is no overlap between voltage and current waveforms; regarding condition (7b), it is fulfilled zeroing the cosine terms, i.e. making φ_n-ψ_n=$\pi/2$. To this goal, voltage (V_n) and current (I_n) components are related by purely reactive elements, represented by a parallel R-C combination at fundamental frequency and a capacitive loading at all harmonics [7].

The approaches above have different circuit implementation and complexity, since for the Class F the output network is designed to synthesise open or short circuit terminations at odd or even frequency harmonics respectively, by a huge number of idlers (increase in circuit complexity). On the contrary, in Class E approach, output network design is simpler, requiring few elements [7].

When operating frequency enters the microwave range, both ideal Class E and F strategies degrade their performances, due to the difficult realization of the idlers (Class F) and to the active device output capacitive behavior, practically shorting higher components and not allowing therefore the desired wave shaping. To infer useful design criteria it is necessary to start from conditions (7), accounting for the limitations mentioned above. The number of controllable harmonics must be limited to the second and third ones, due also to practical implementation and feasibility constraints. With such hypotheses, a new practical approach (Harmonic Manipulation, HM) for the design of harmonic-tuned amplifiers has been recently suggested in [3]. In this case, assuming the active device output acting as a current source voltage-controlled by the external input signal P_{in}, the output drain voltage waveform can be shaped through a proper choice of the output harmonic terminations. To obtain simplified expression and to infer design guidelines, purely resistive output terminations have been considered, shorting higher harmonics. Thus, the drain voltage waveform obtainable controlling up to 3f, becomes :

$$v_{ds}(t) = V_{DD} - V_1 \cdot \begin{bmatrix} \cos(\omega t) + k_2 \cdot \cos(2\omega t) \\ +k_3 \cdot \cos(3\omega t) \end{bmatrix} \quad (8)$$

where

$$k_2 = \frac{V_2}{V_1} \quad , \quad k_3 = \frac{V_3}{V_1} \quad (9)$$

As a consequence, the optimisation of η is equivalent to finding k_2 and k_3 values that maximise V_1, with the boundary condition $0 \le v_{ds}(t) \le V_{BD}$ where V_{BD} is the

breakdown voltage and 0V has been assumed for the knee voltage. Results [3] are briefly summarised in TABLE 1.

TABLE 1
RESULTS OBTAINABLE WITH OPTIMISED HARMONIC TERMINATIONS

controlled frequencies	k_2	k_3	δ	V_1 increase
f (TL)	0	0	1	$V_{1,TL}=V_{DD}$
f , 2f , 3f (FG)	-0.55	0.17	1.62	$V_{1,FG}=1.62\cdot V_{DD}$

In this table, the *Voltage Gain Function* δ is defined as

$$\delta(k_2,k_3)=\frac{V_1}{V_{DD}} \qquad (10)$$

It relates the fundamental drain voltage amplitude V_1, obtainable by proper harmonic terminations (k_2,k_3), to the bias voltage V_{DD}, that can be considered as the fundamental amplitude for the unmanipulated approach, i.e. for the Tuned Load case (TL, implying short-circuit termination at all harmonics).
Assuming drain current harmonics unaffected by output terminations, the δ function directly gives the improvement in drain efficiency with respect to the unmanipulated case (TL). However, the values for δ have to be considered carefully, not to violate physical constraints. In fact, since the drain voltage harmonic components V_n are generated by the current harmonic components I_n through the impedances Z_n (eqn.2), it is necessary to verify that k_2 and k_3 optimum values can be physically synthesised, i.e. that the corresponding impedances Z_2 and Z_3 have real positive values. To this goal, current harmonic components I_2 and I_3 have to satisfy proper phase relationships with respect to I_1 (see TABLE 1, signs of k_2 and k_3). Such phase relationships are important and the lack in their fulfillment leads to detrimental results.
Optimum load impedances for the intrinsic drain current source are determined as

$$\begin{aligned} R_f &= \delta(k_2,k_3)\cdot\frac{V_{DD}}{I_1} \\ R_{2f} &= \delta(k_2,k_3)\cdot k_2\cdot\frac{V_{DD}}{I_2} \\ R_{3f} &= \delta(k_2,k_3)\cdot k_3\cdot\frac{V_{DD}}{I_3} \end{aligned} \qquad (11a)$$

The HM approach can be useful if the generated drain current waveform allows positive values for R_{nf}, according to eqn (11). In this case, even if there is a power dissipation on the harmonic loads, that could be interpreted a detrimental phenomena, the fundamental output power is maximised, thus maximising drain efficiency too. It is to note that if the same analysis were applied with the aim to minimise the dissipated power, only sub-optimum results could be obtained [4]. Different approaches proposed in literature are in fact based on the partial assumption that efficiency maximisation is equivalent to the reduction of the dissipated power on the active device, even if the number of harmonics that can be controlled is necessarily reduced [4]. The same criteria (P_{diss} minimisation) have been applied for high frequency Class E amplifier [8]. Even if the C_{ds} and G_{ds} components are not considered in this simplified analysis, the results of the HM approach are related to the output harmonic terminations and to the drain current waveform. Input harmonic loading becomes therefore crucial to control the drain current components generation mechanism [9].

IV. Design Examples and Remarks

To validate the above statements, two single stages PAs have been designed following different criteria. The first one is a Class E amplifier, while the second is a Class FG one. The active device used is a medium power GaAs MESFET (0,5 μm gate length, 1mm periphery) by AMS with a Class AB bias (≈30% I_{max}), V_{DD}=5V @f=5GHz. For the two amplifiers, input networks have been designed to assure an input matching condition (Class E) or to generate the output drain current harmonic components with a proper phase relationship, according to TABLE 1 (Class FG). The output networks have been designed respectively according to Class E or HM strategies (eqn(11)). The layouts of the two designed amplifiers are shown in Fig.2.

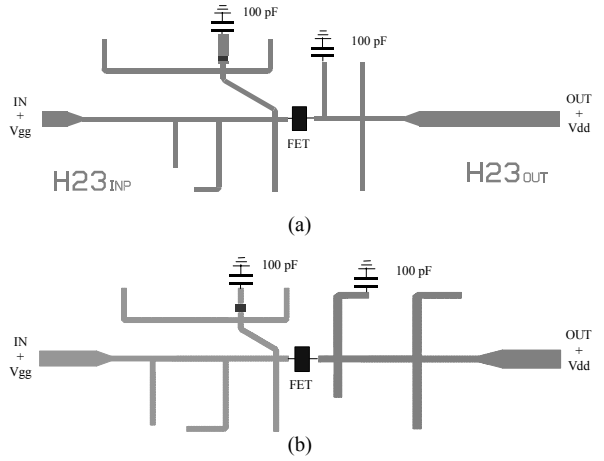

Fig.2: Layouts for the Class FG (a) and Class E (b) designs

Simulated output power and power added efficiency for both amplifiers are shown in Fig.3 and Fig.4 respectively, together with measured performances for the realised Class FG PA. As it can be noted, Class FG amplifier assures a higher output power and efficiency at 1dB compression with respect to the Class E design.

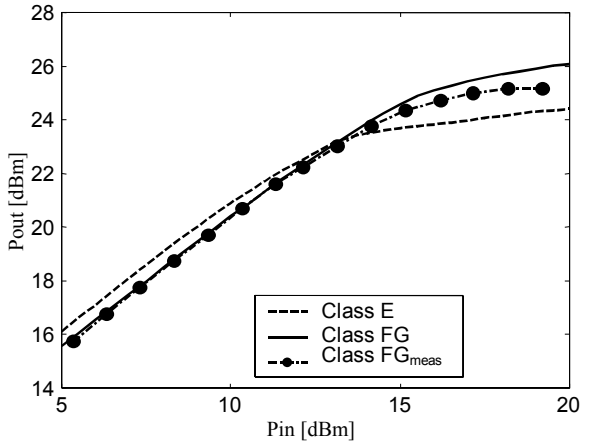

Fig.3: P_{out} simulated for the Class FG (solid), Class E (dotted) and measured for the realised Class FG (dashed-dotted) designs.

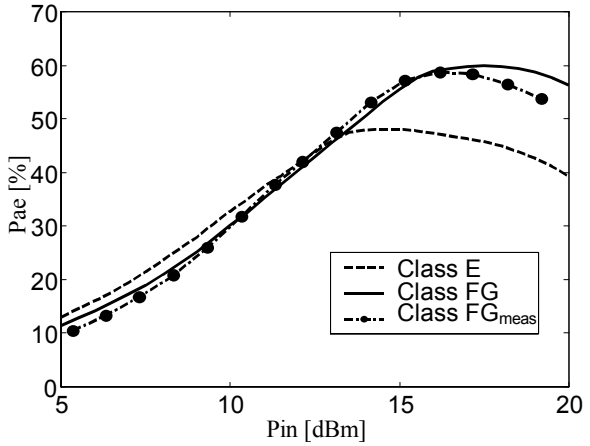

Fig.4: η_{add} simulated for the Class FG (solid), Class E (dotted) and measured for the realised Class FG (dashed-dotted) designs.

V. Conclusions

Power balance considerations have been discussed, with a major impact in potential performances, stressing the relevance of the power dissipated at harmonic frequencies.

The high frequency operation of two different strategies for high efficiency PA design have been considered, respectively Class E and Class FG, and their performances have been compared by means of test design examples performed on a single-stage power amplifier operating at 5 GHz.

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